

FIGURE 1B

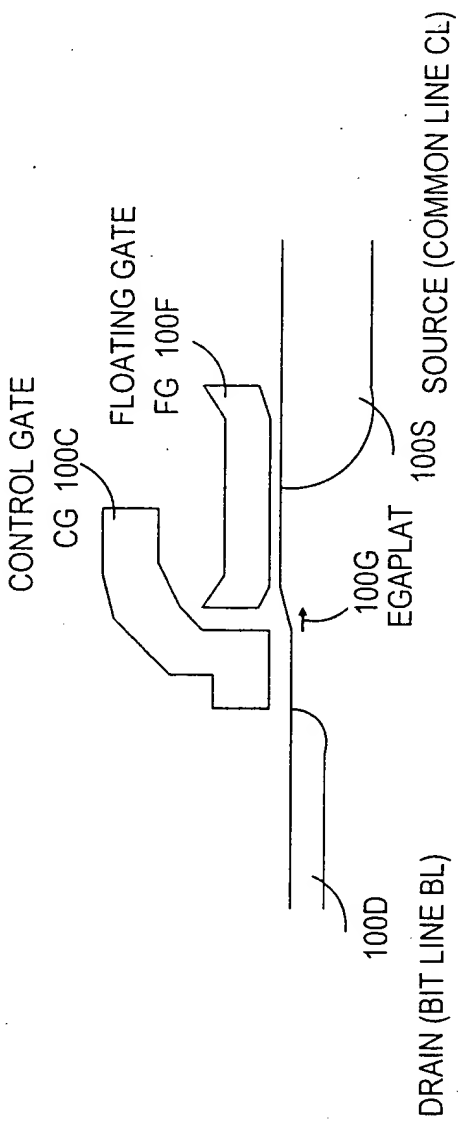
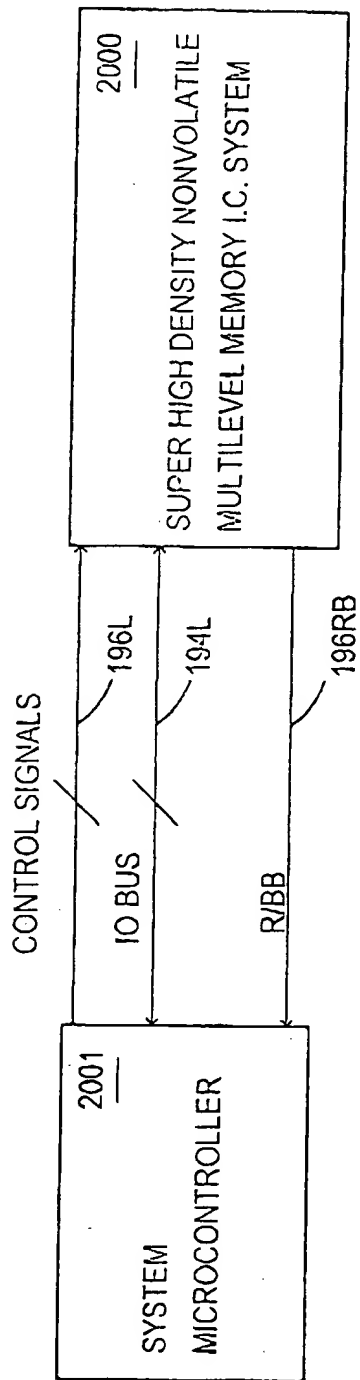


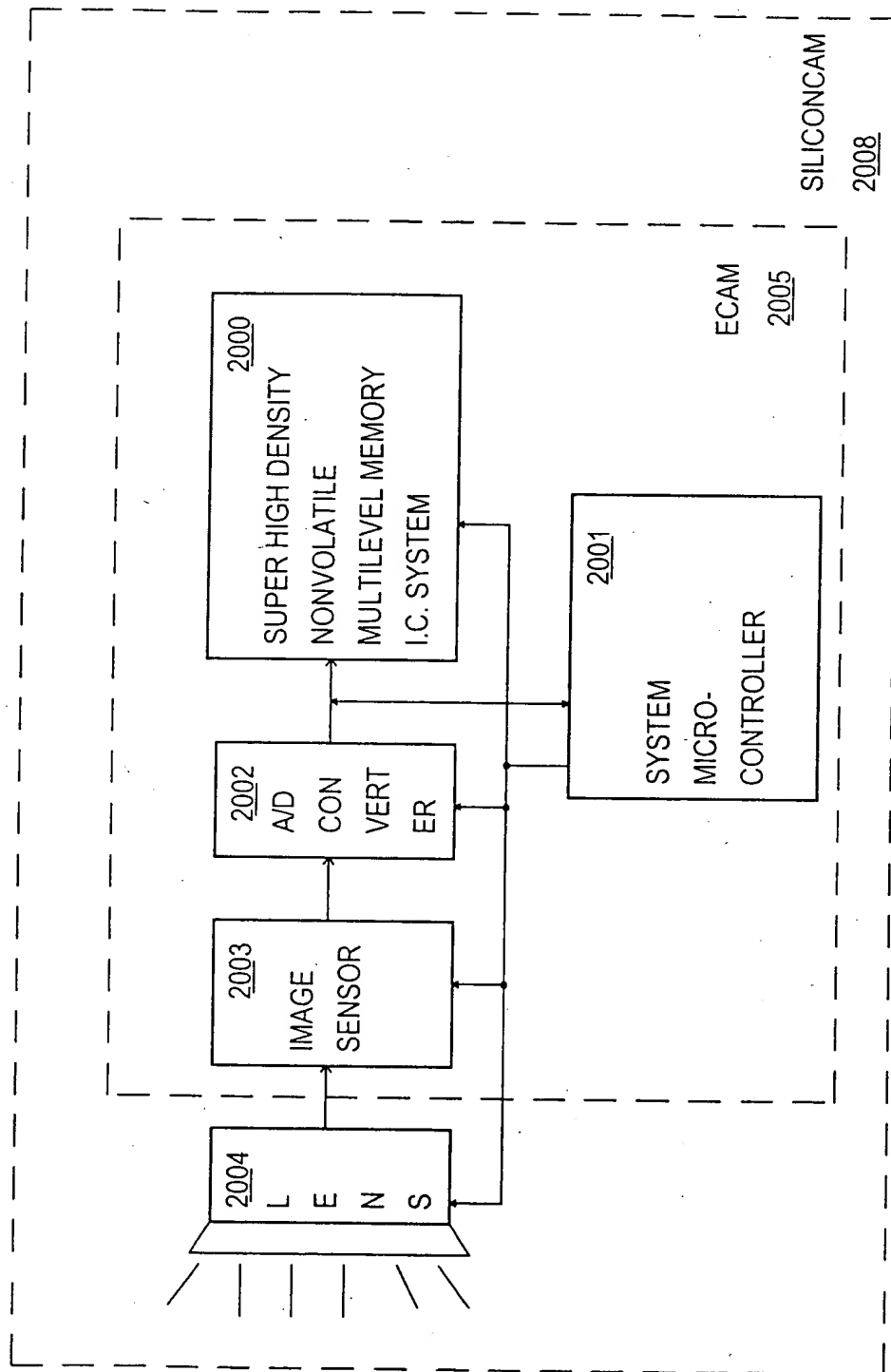
FIGURE 1A

SOURCE SIDE INJECTION FLASH MEMORY CELL: CROSS SECTION ALONG THE BIT LINE



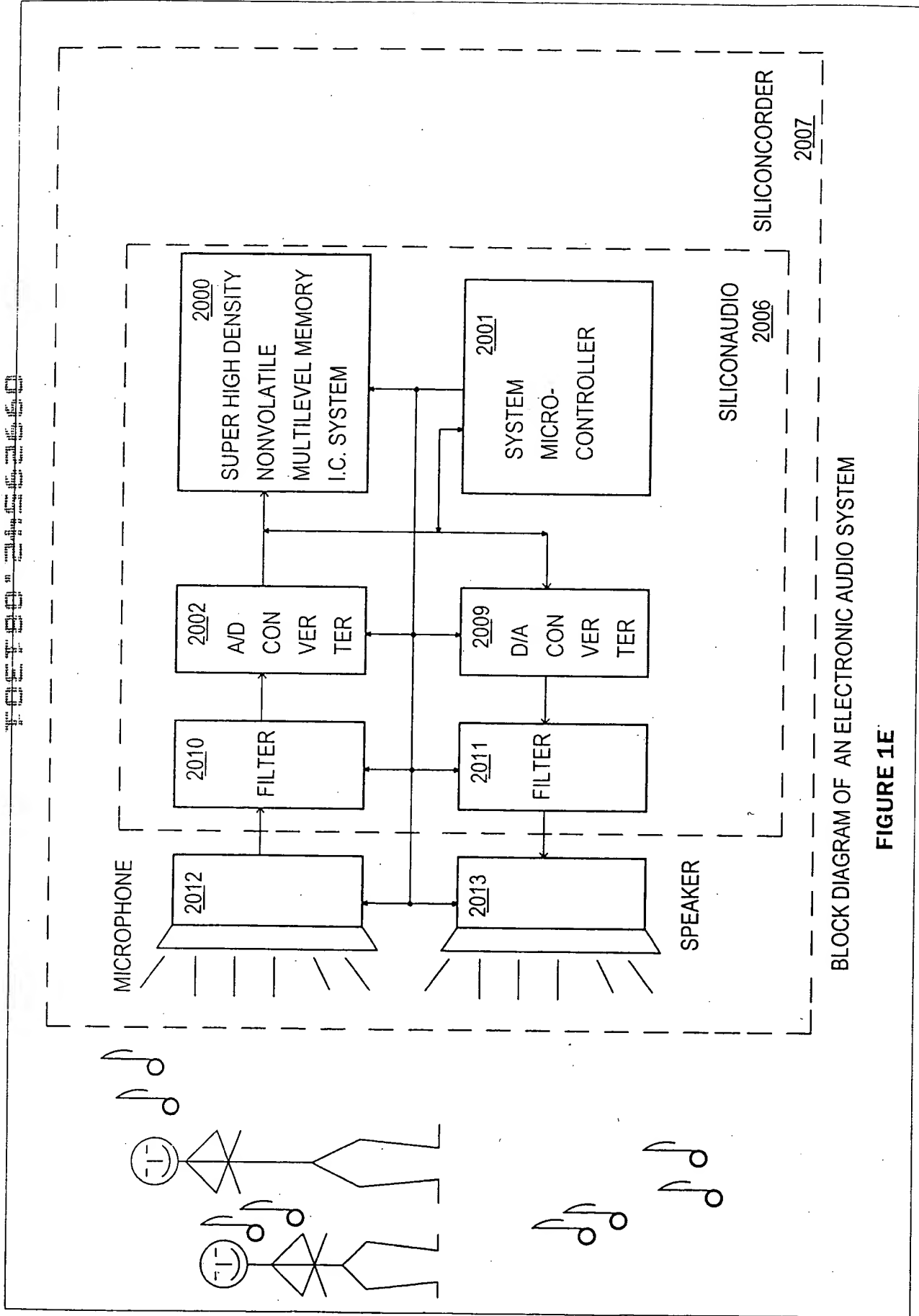
BLOCK DIAGRAM OF A NONVOLATILE MULTILEVEL MEMORY SYSTEM

FIGURE 1C



BLOCK DIAGRAM OF AN ELECTRONIC CAMERA SYSTEM

FIGURE 1D



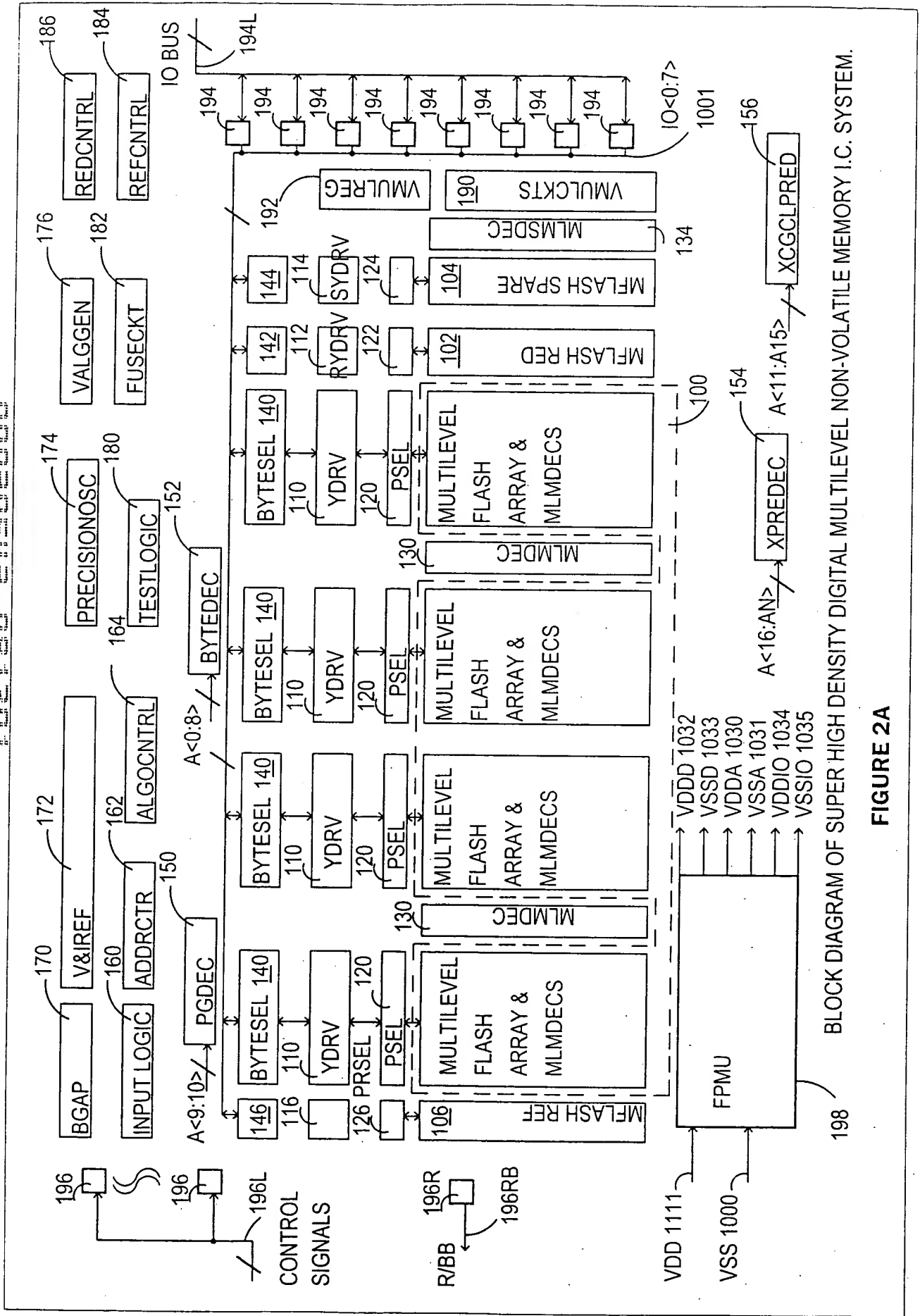


FIGURE 2A

BLOCK DIAGRAM OF SUPER HIGH DENSITY DIGITAL MULTILEVEL NON-VOLATILE MEMORY I.C. SYSTEM.

REF ID: A4562660

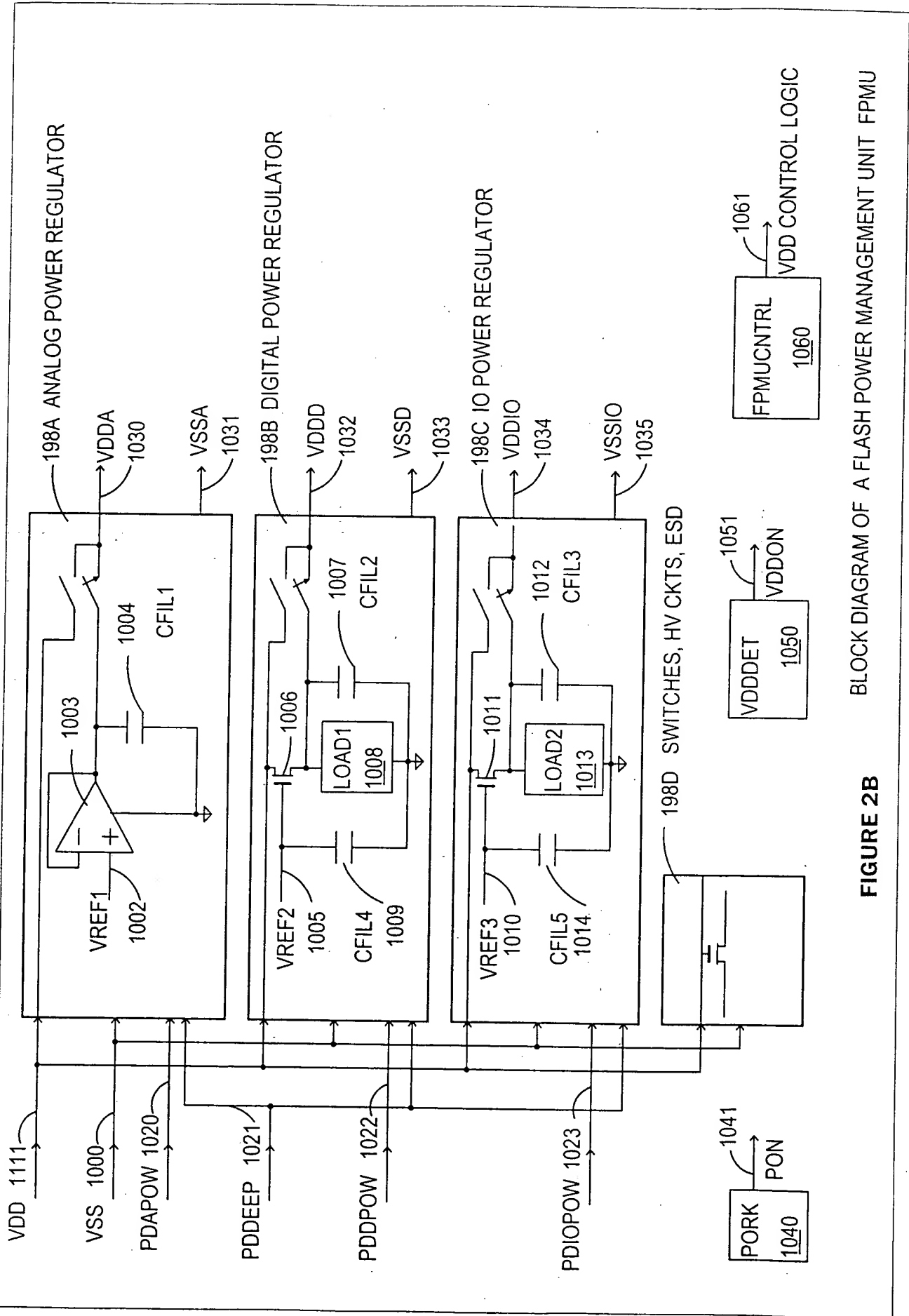
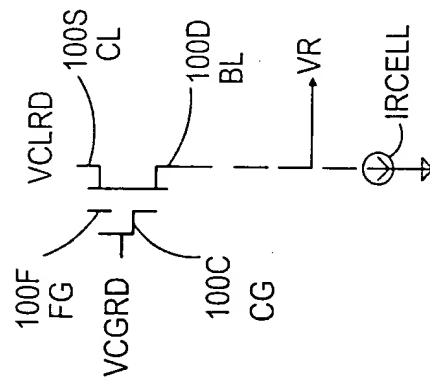
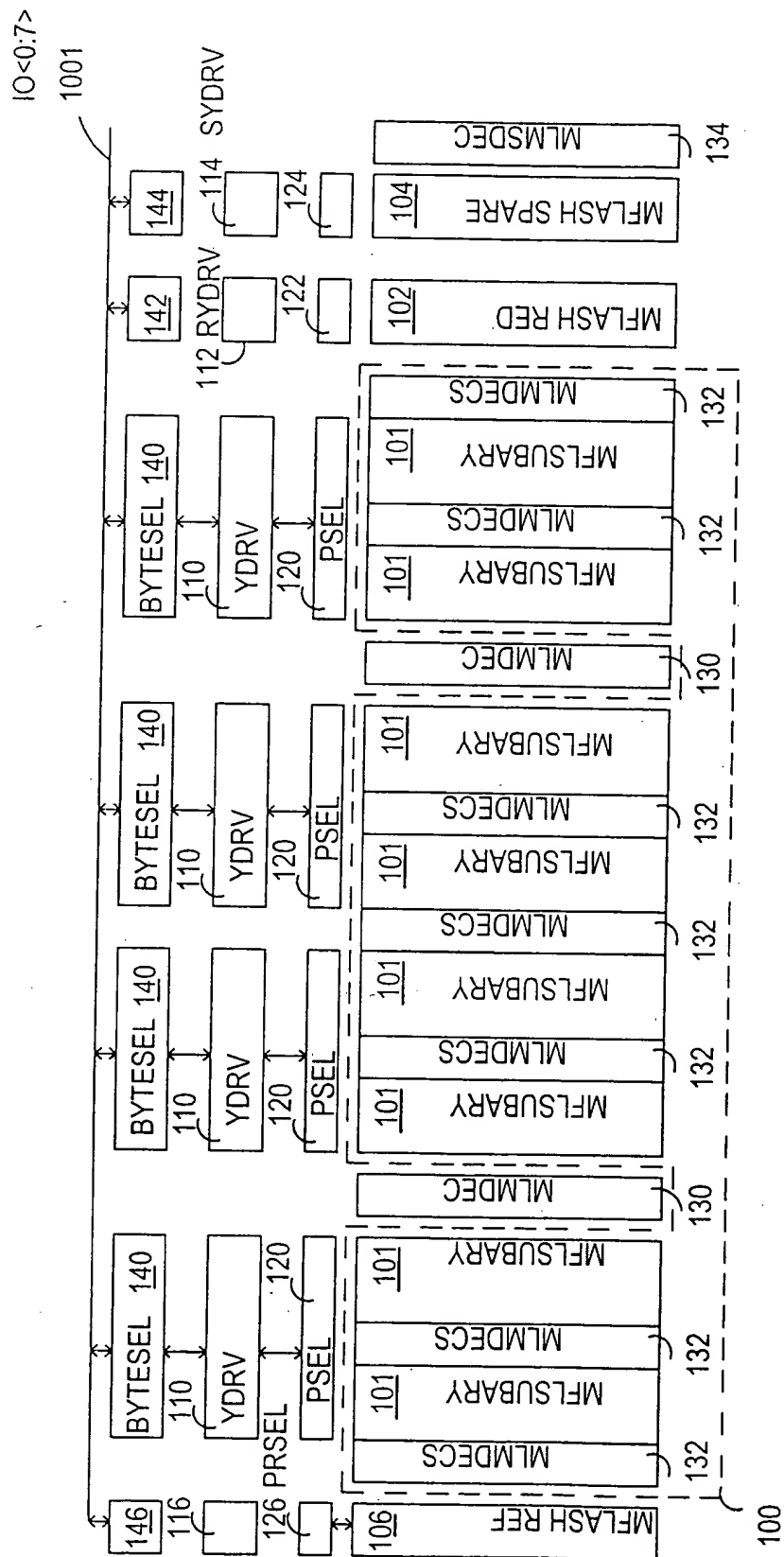


FIGURE 2B BLOCK DIAGRAM OF A FLASH POWER MANAGEMENT UNIT FPMU



VOLTAGE MODE SENSING

FIGURE 2C



**FIGURE 3A**



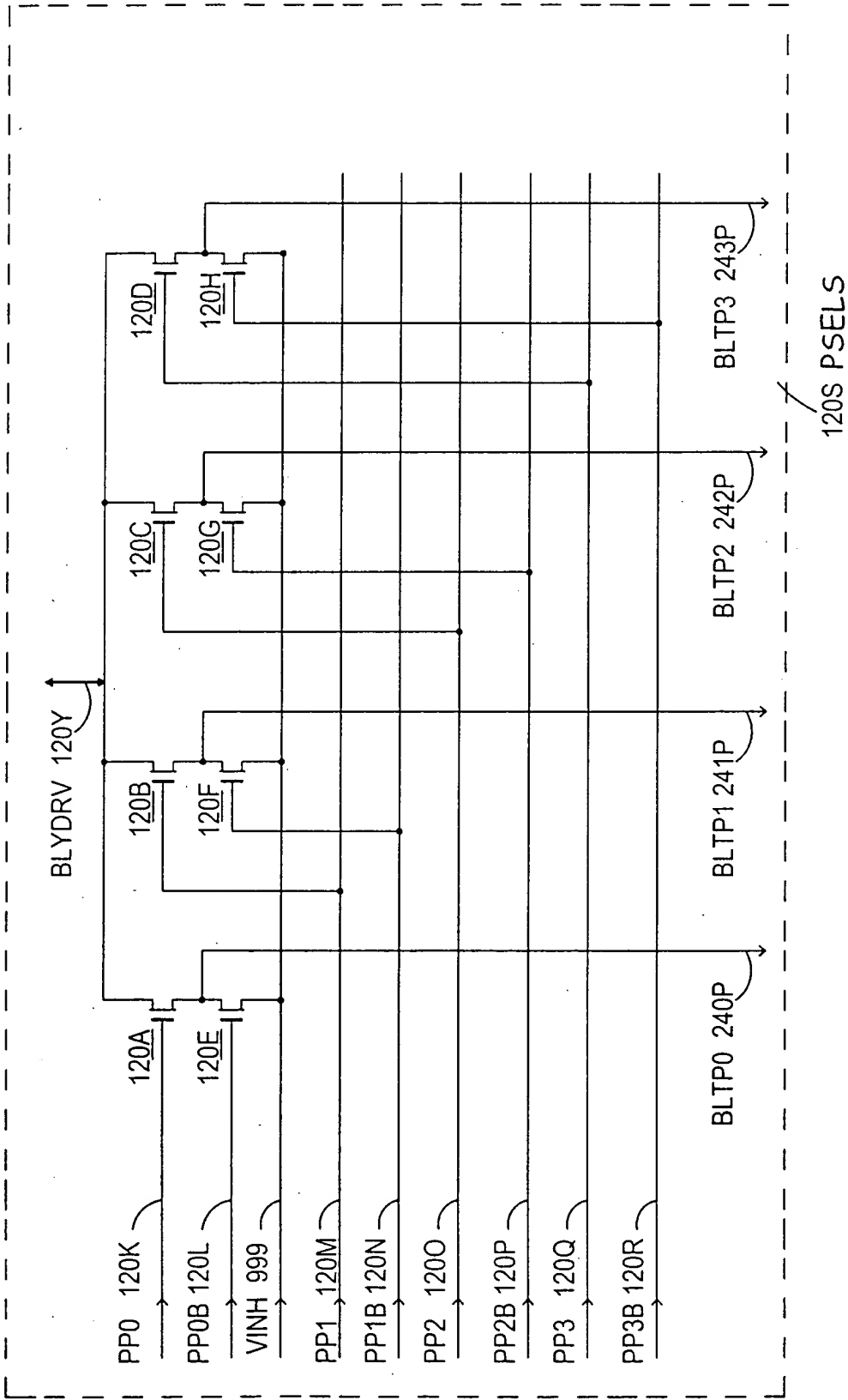


FIGURE 3B

FIG. 3C

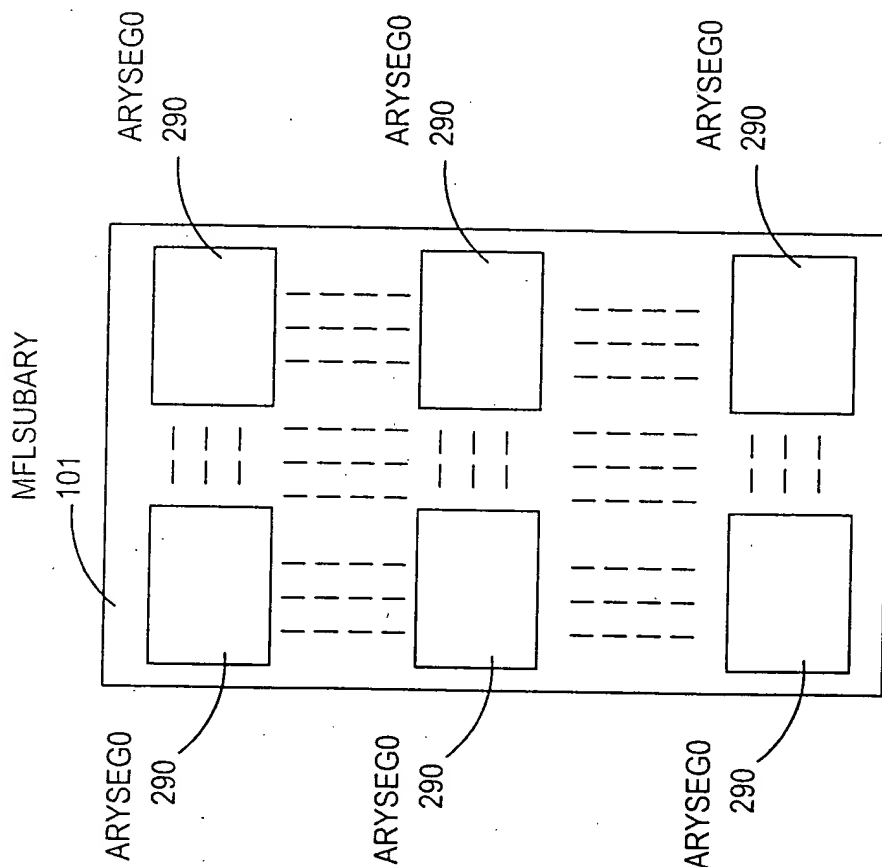
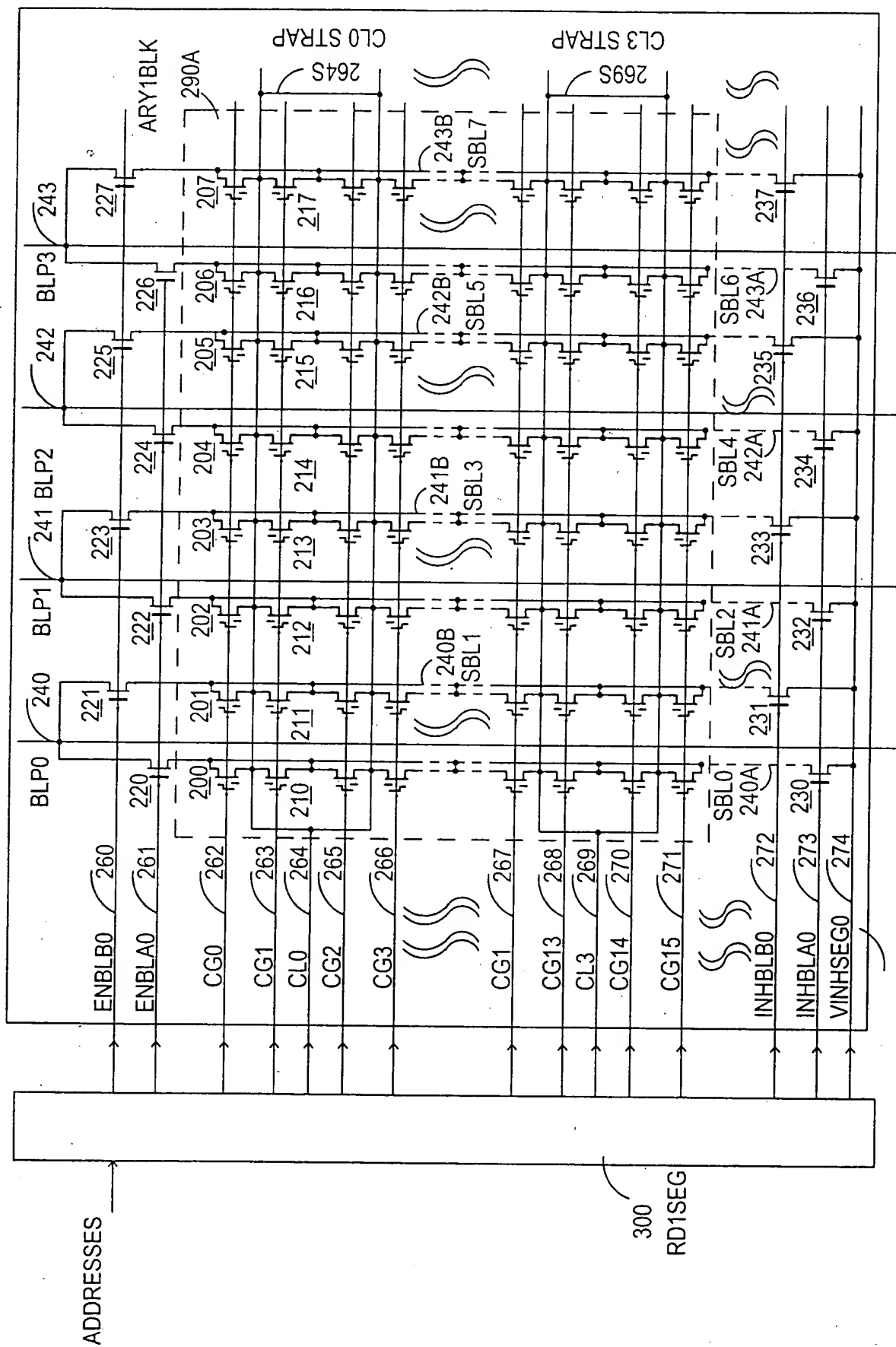


FIGURE 3C



## INHIBIT AND SELECT SCHEME

290 ARYSEGO

FIGURE 4B

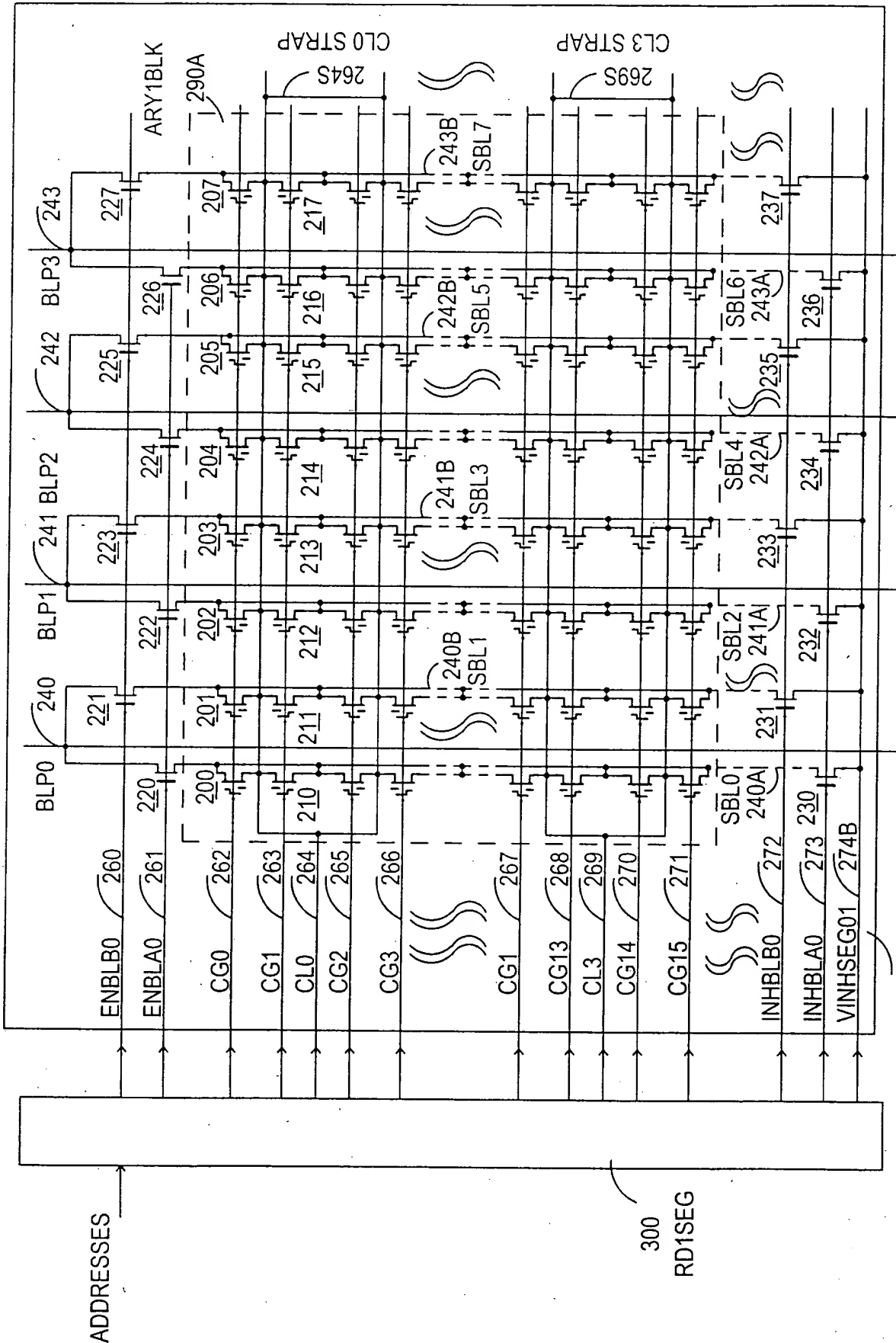


FIGURE 4B INHIBIT AND SELECT SCHEME

# INHIBIT AND SELECT SCHEME

**FIGURE 4C**

290 ARYSEG0

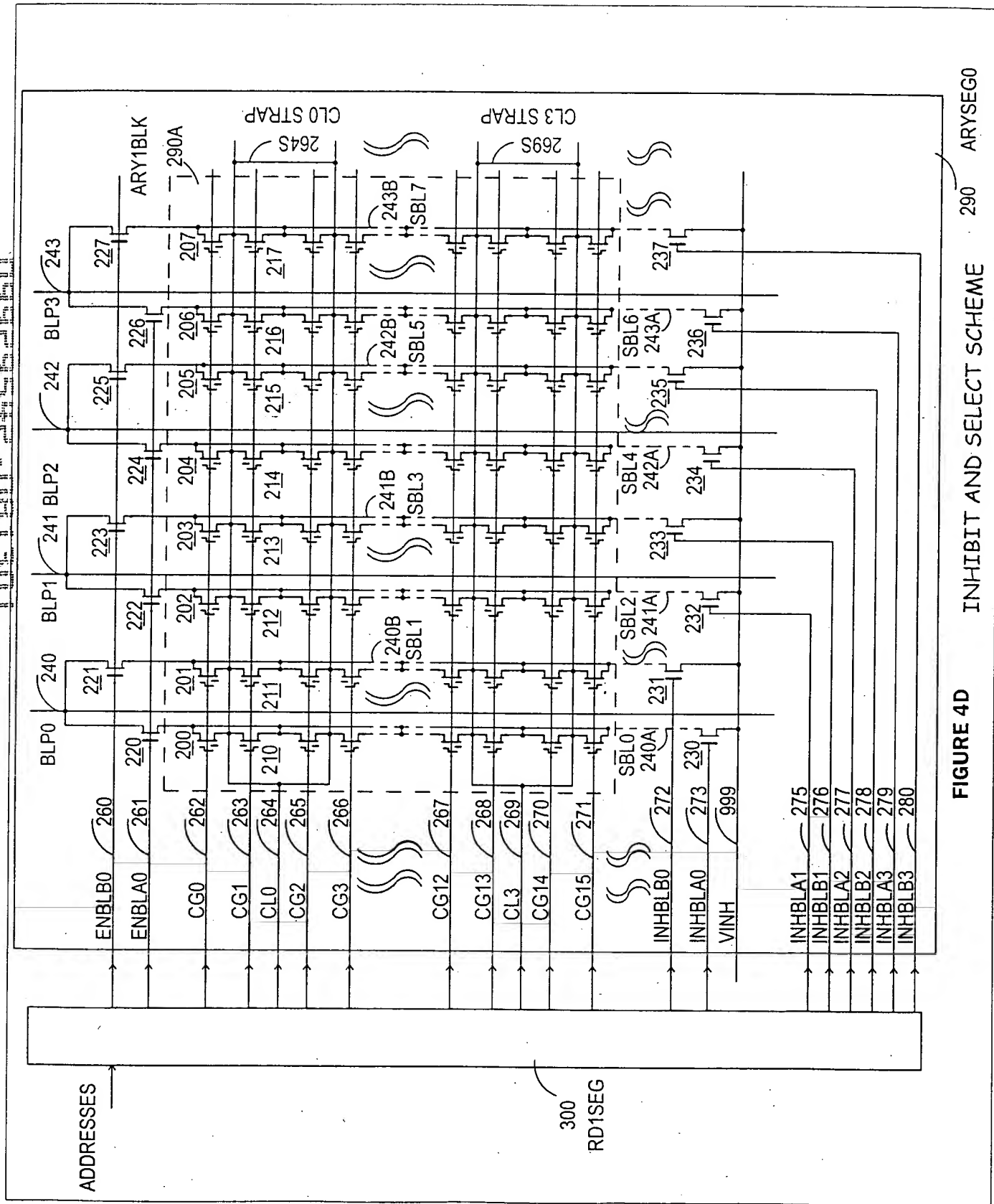


FIGURE 4D INHIBIT AND SELECT SCHEME 290 ARYSEGO

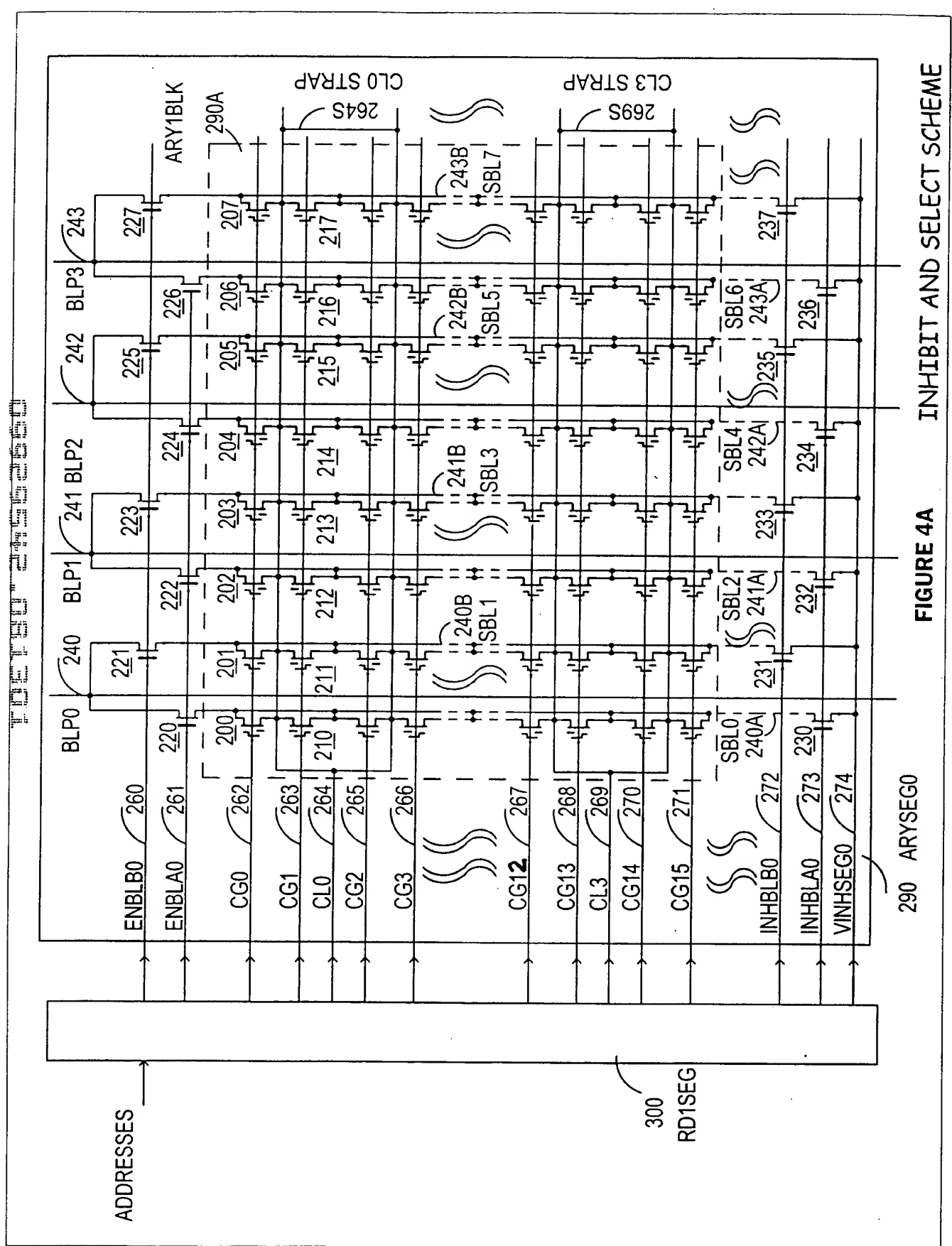
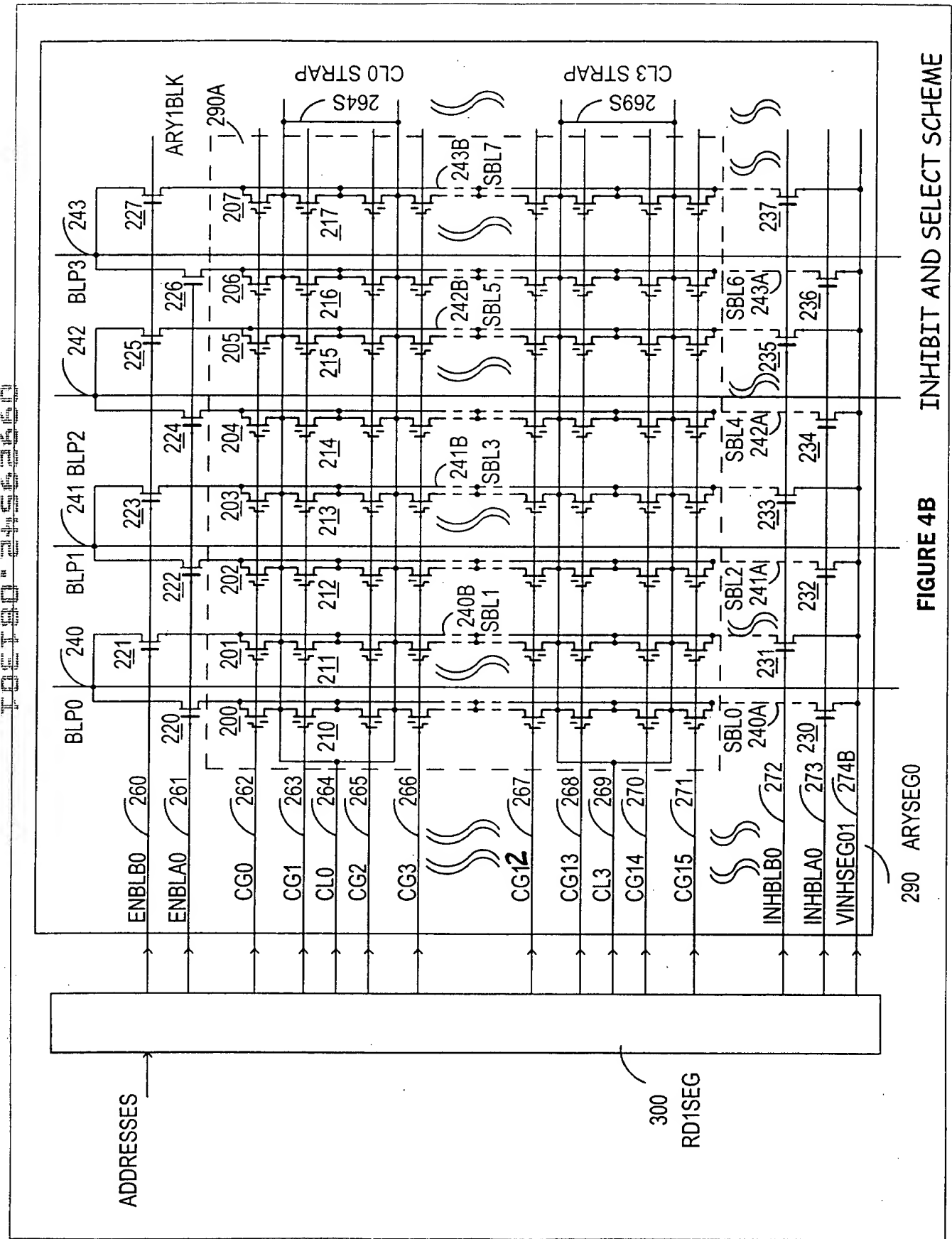


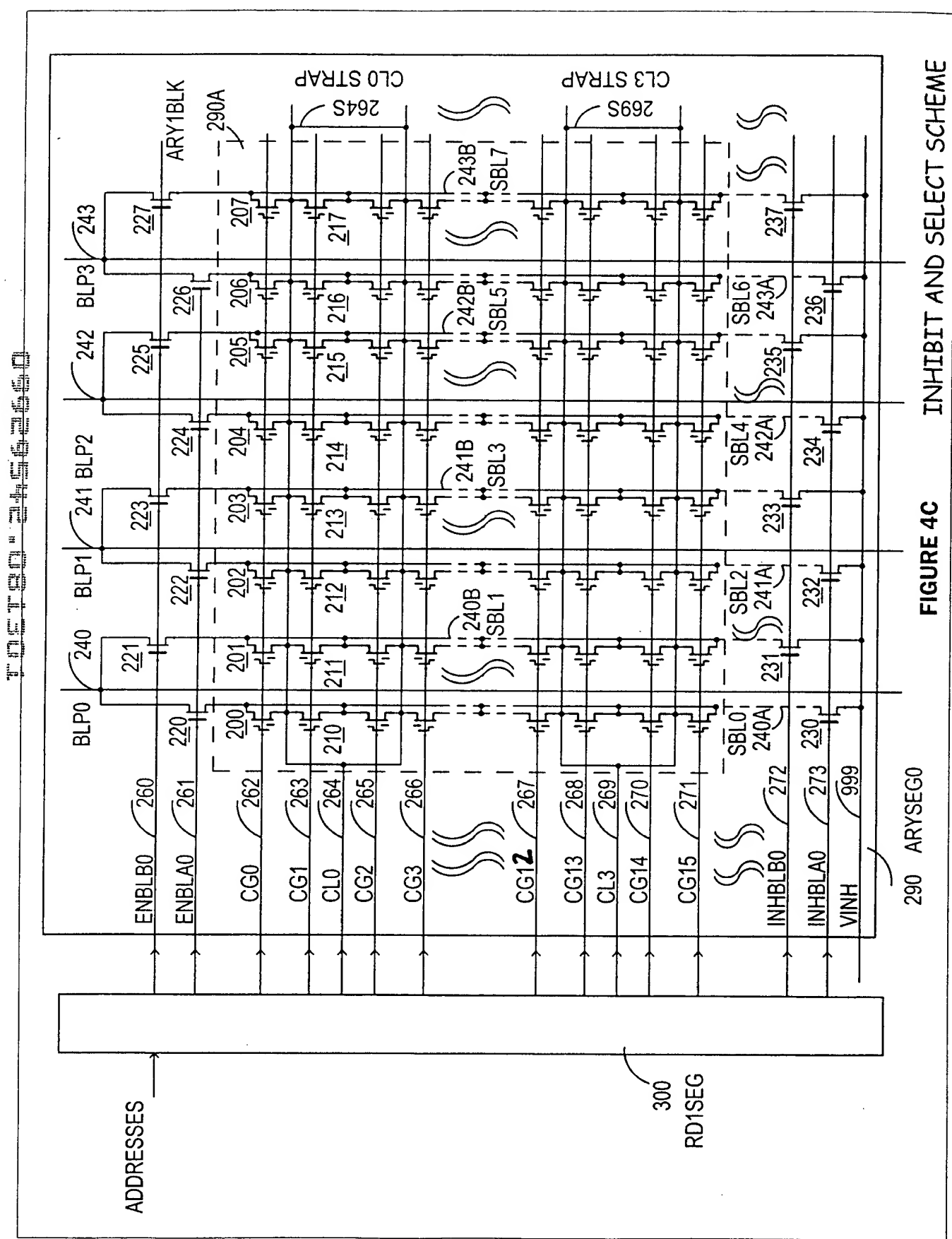
FIGURE 4A INHIBIT AND SELECT SCHEME

290 ARYSEG0

300 RD1SEG







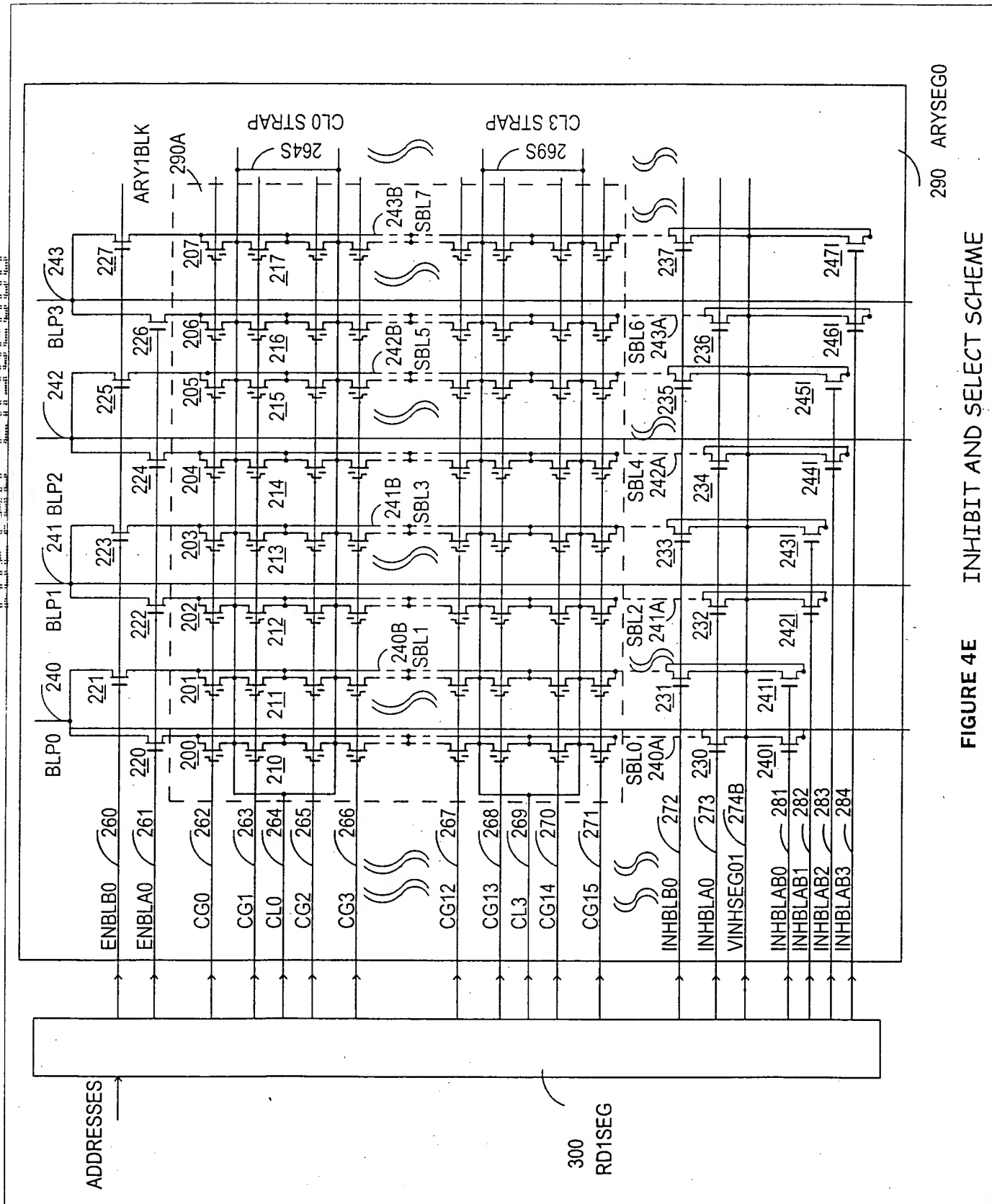


FIGURE 4E INHIBIT AND SELECT SCHEME

290 ARYSEG0

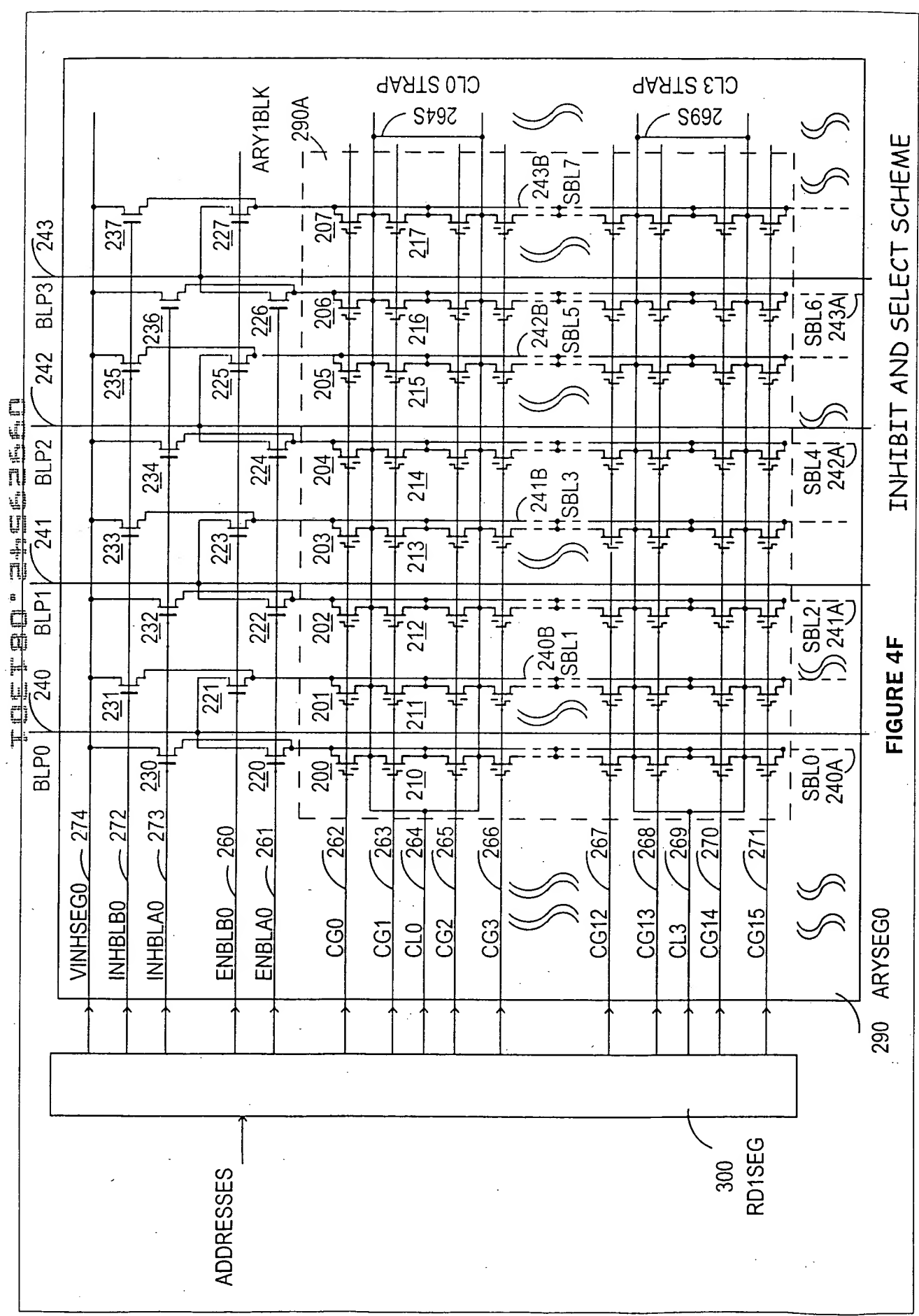
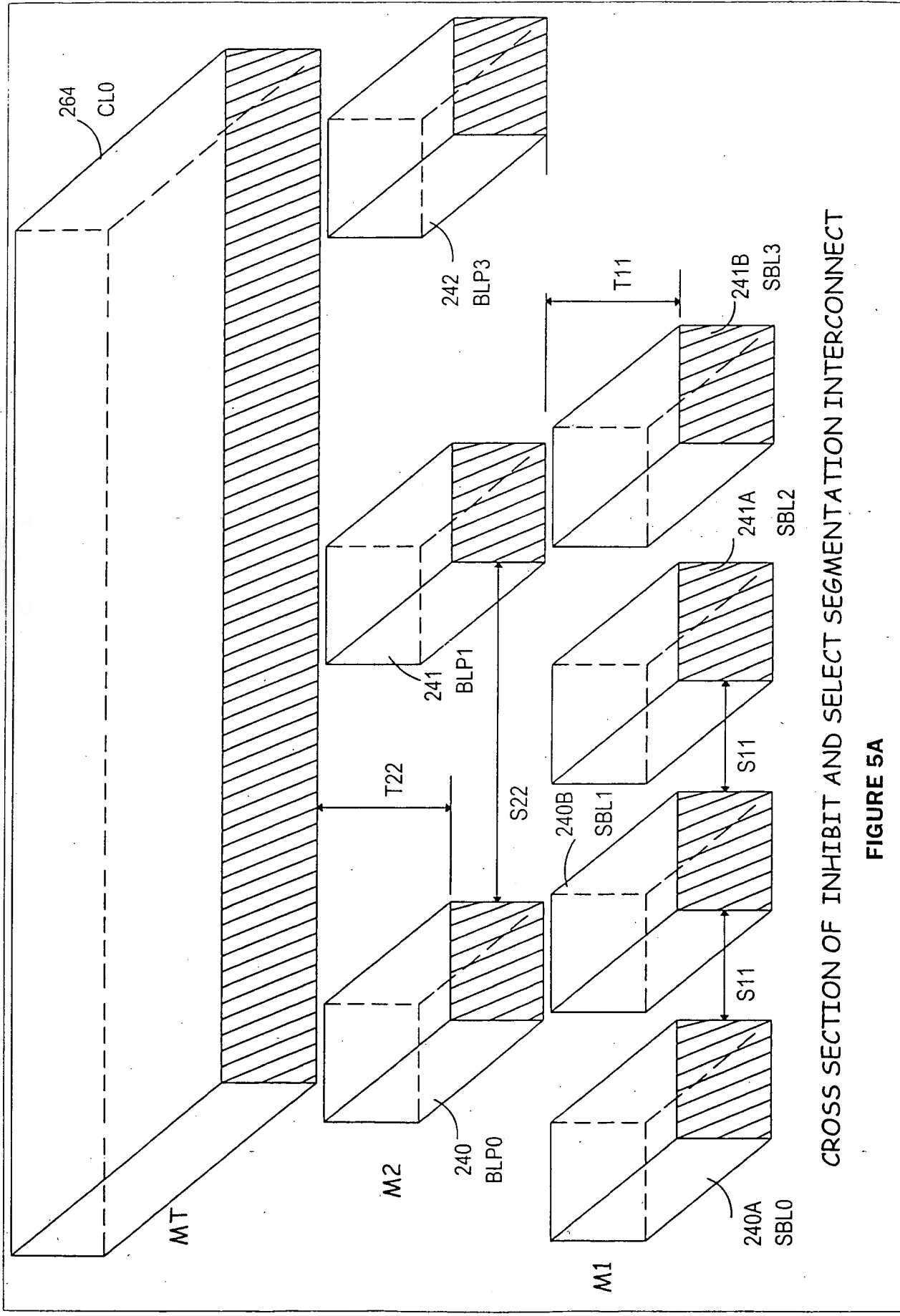


FIGURE 4F INHIBIT AND SELECT SCHEME

TOP VIEW 2462660



CROSS SECTION OF INHIBIT AND SELECT SEGMENTATION INTERCONNECT

FIGURE 5A

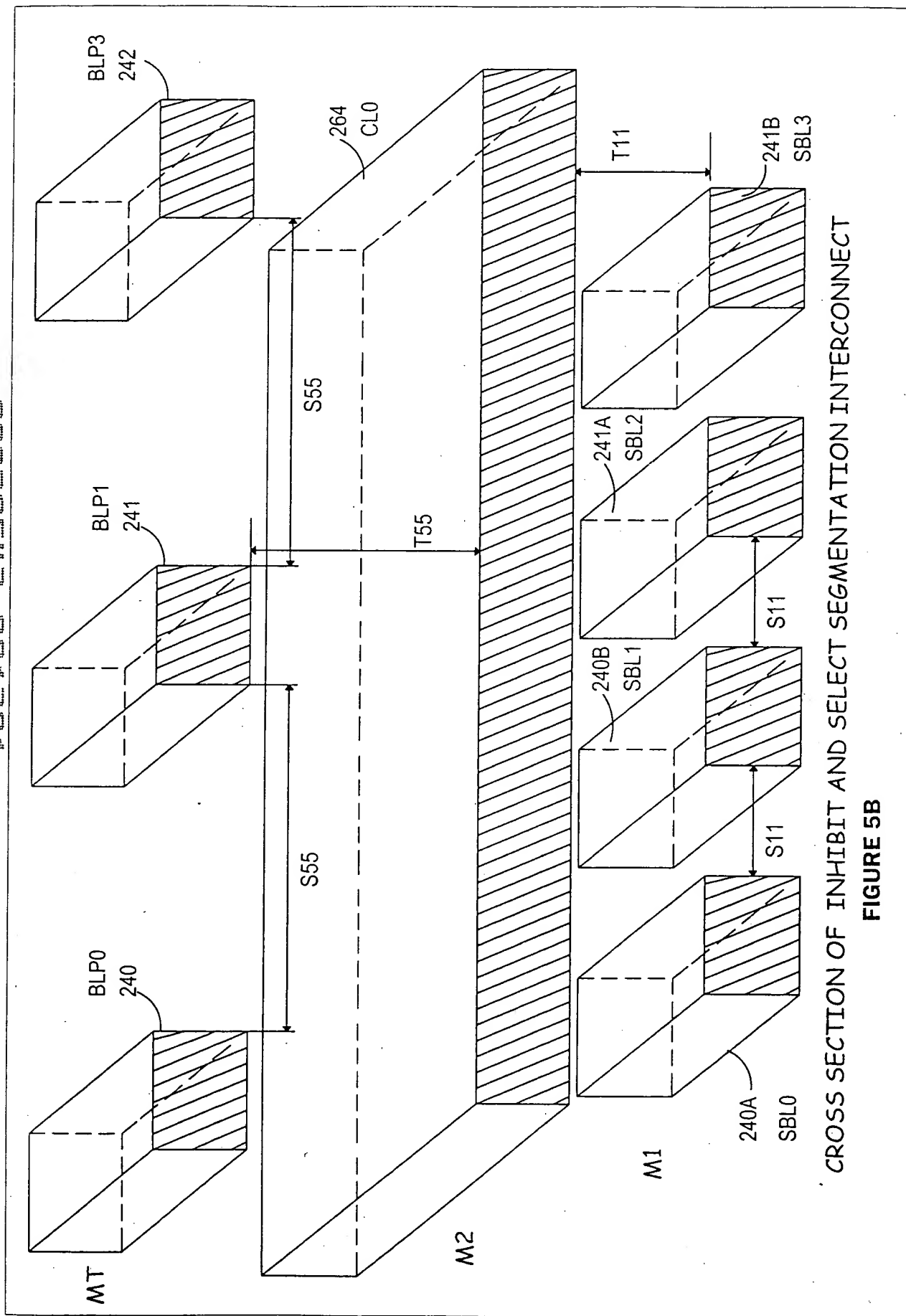
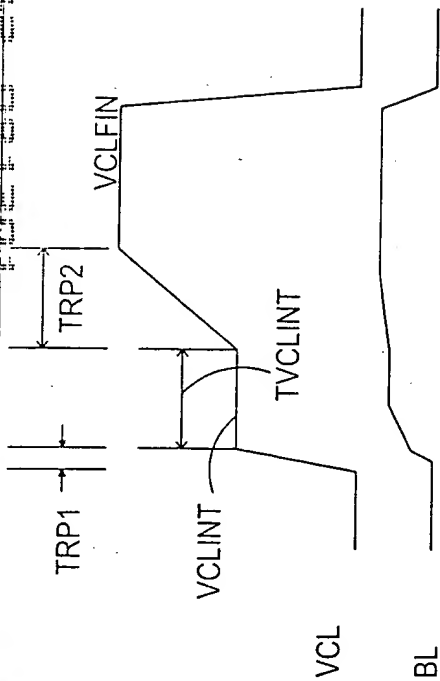
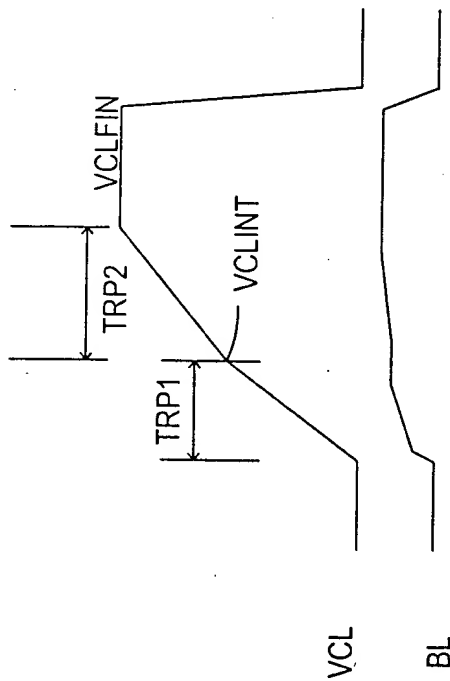


FIGURE 5C

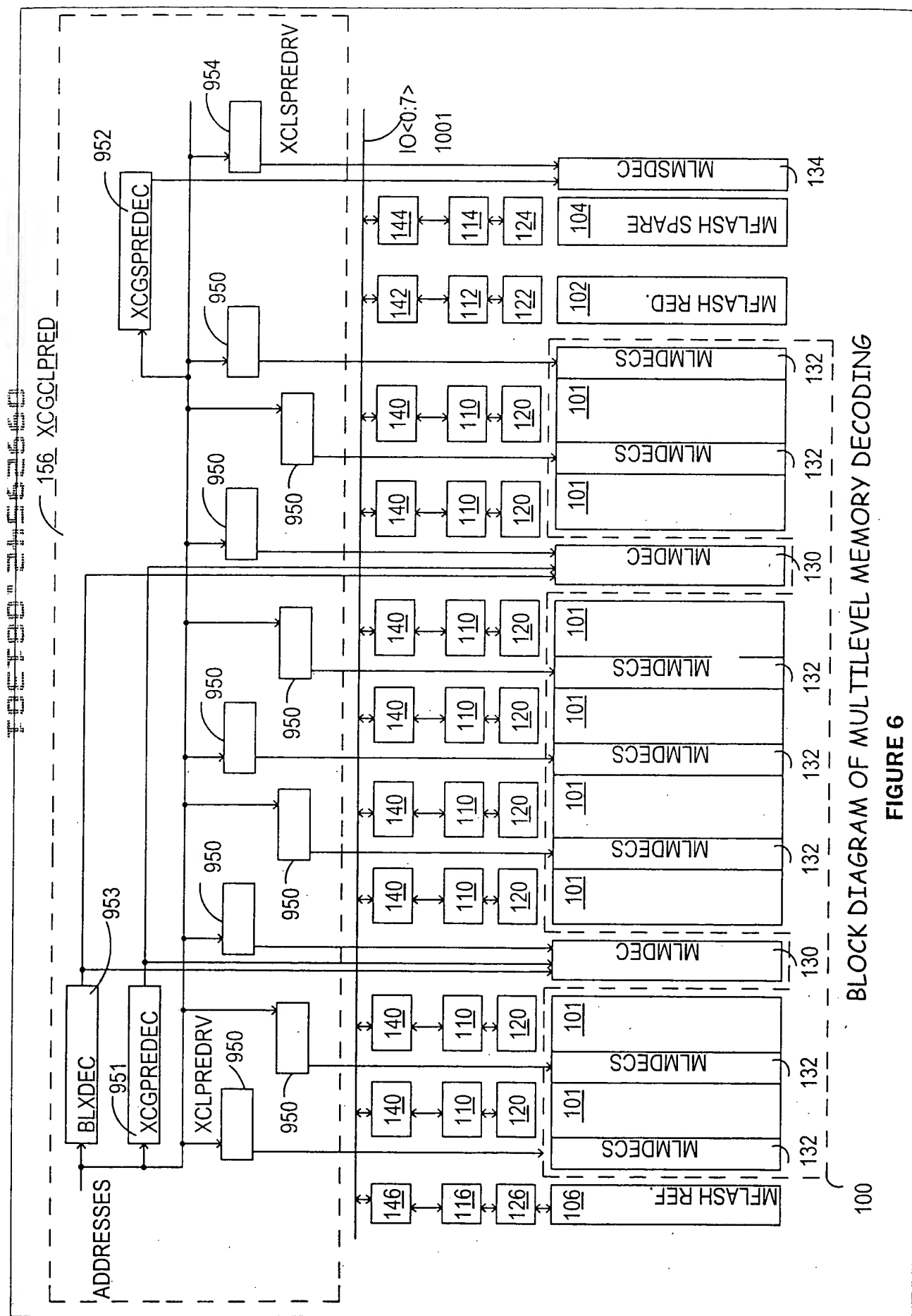


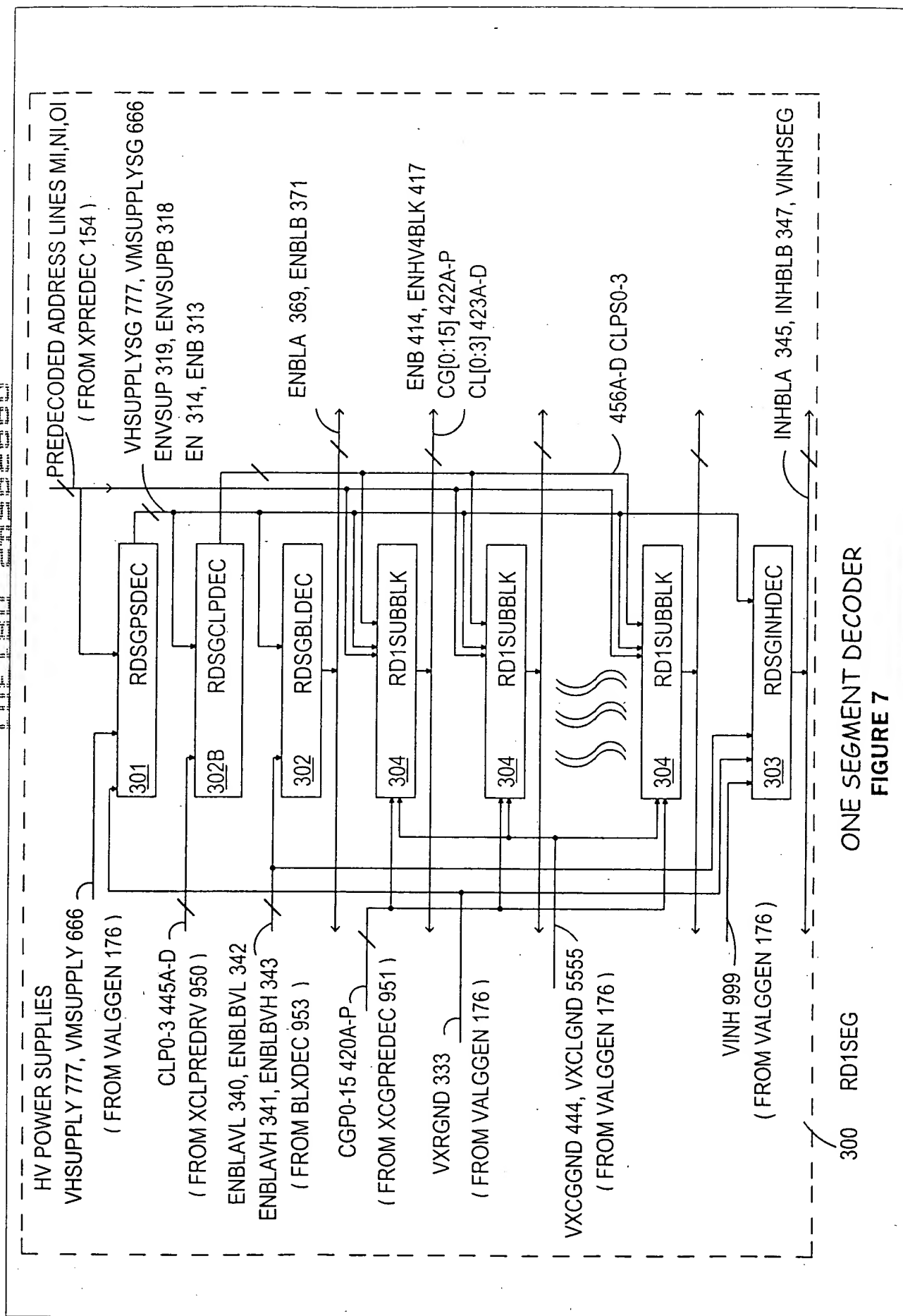
2-STEP RAMP RATE CONTROL



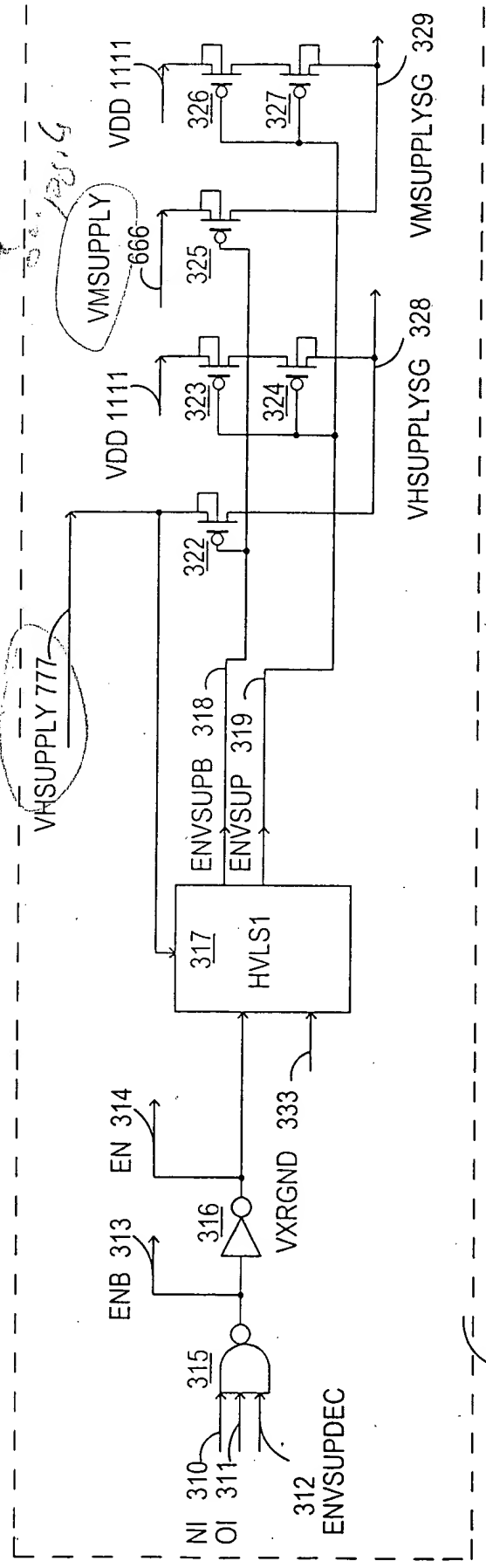
FAST-SLOW RAMP RATE CONTROL

FIGURE 5C









301

RDSGPSDEC

claim 1

SEGMENTED POWER SUPPLY DECODER  
FOR MULTILEVEL MEMORY DECODING

FIGURE 8

FIGURE 9A

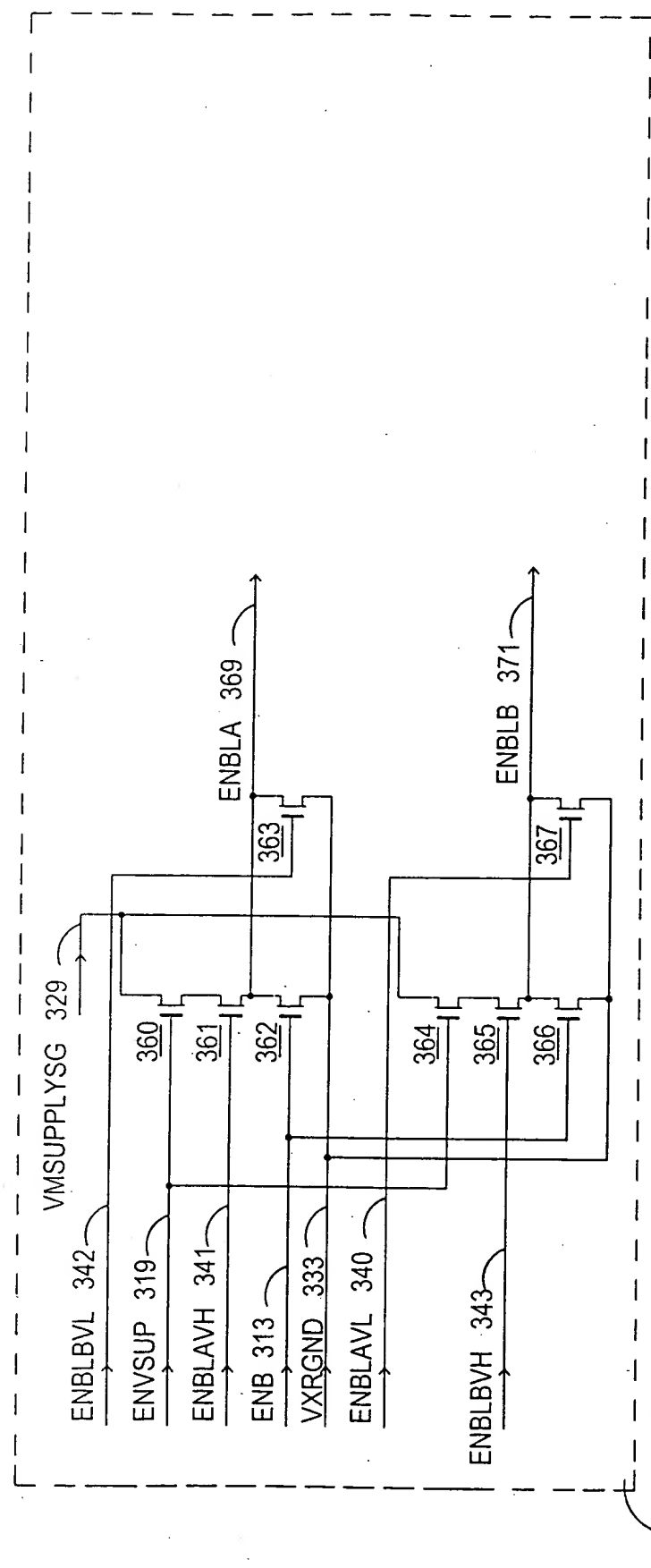


FIGURE 9A  
BL SELECT DECODER FOR  
MULTILEVEL MEMORY DECODING

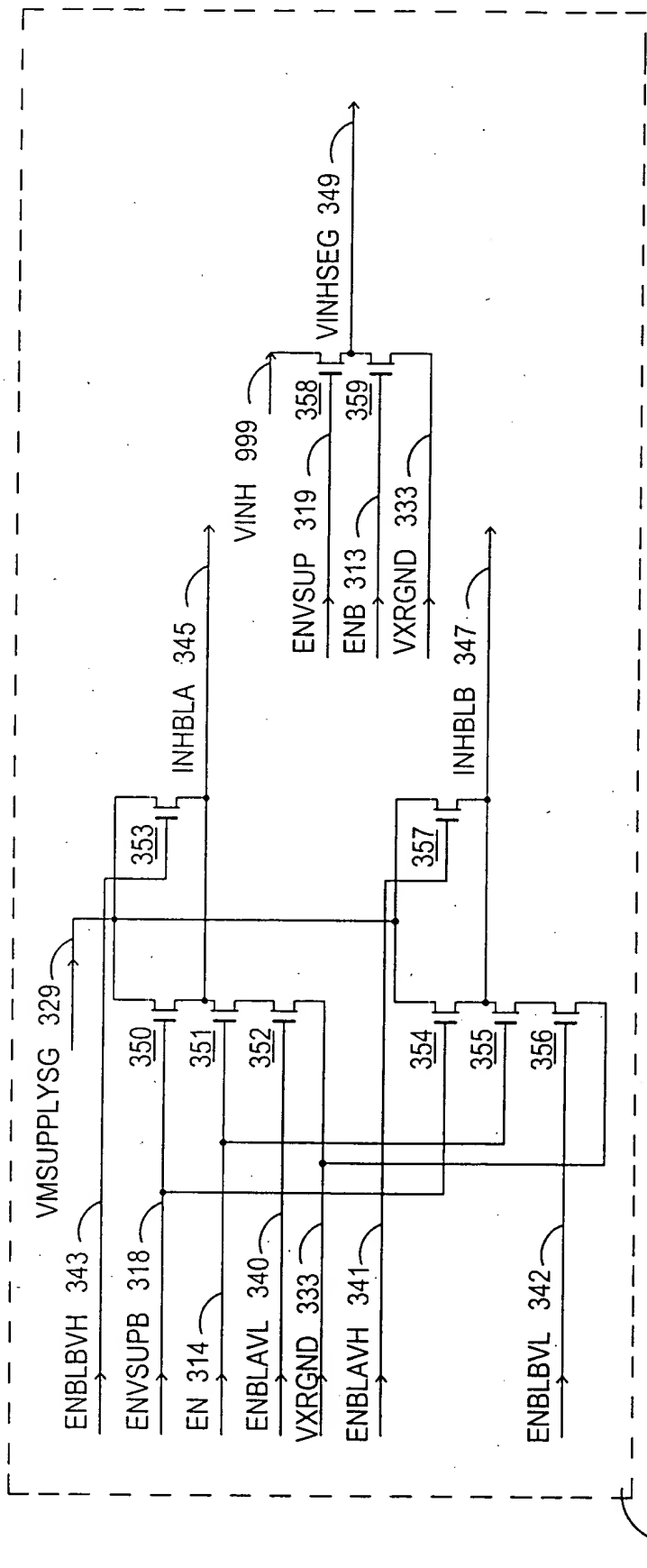


FIGURE 9B INHIBIT DECODER FOR MULTILEVEL MEMORY DECODING

FIGURE 9C

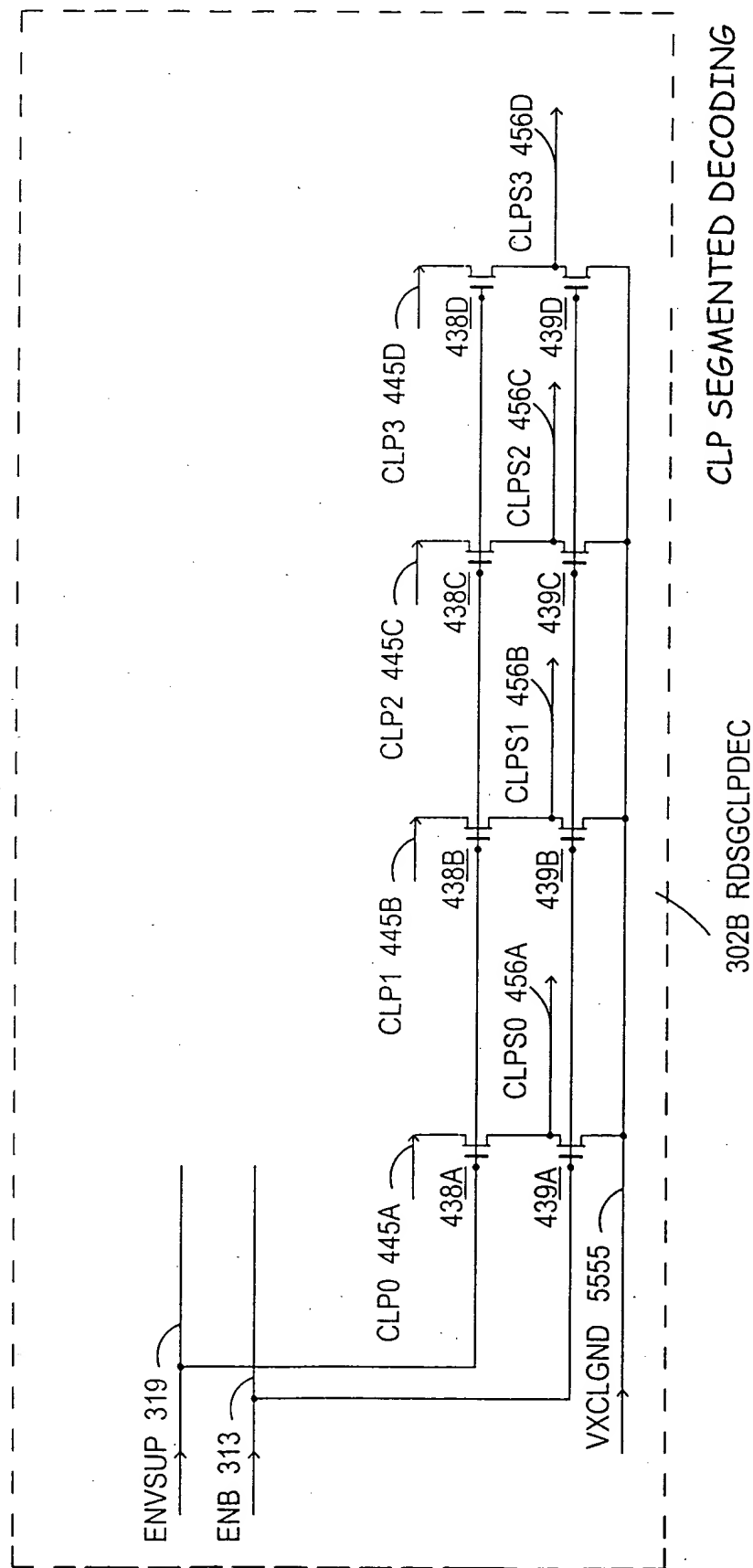


FIGURE 9C

FIGURE 10

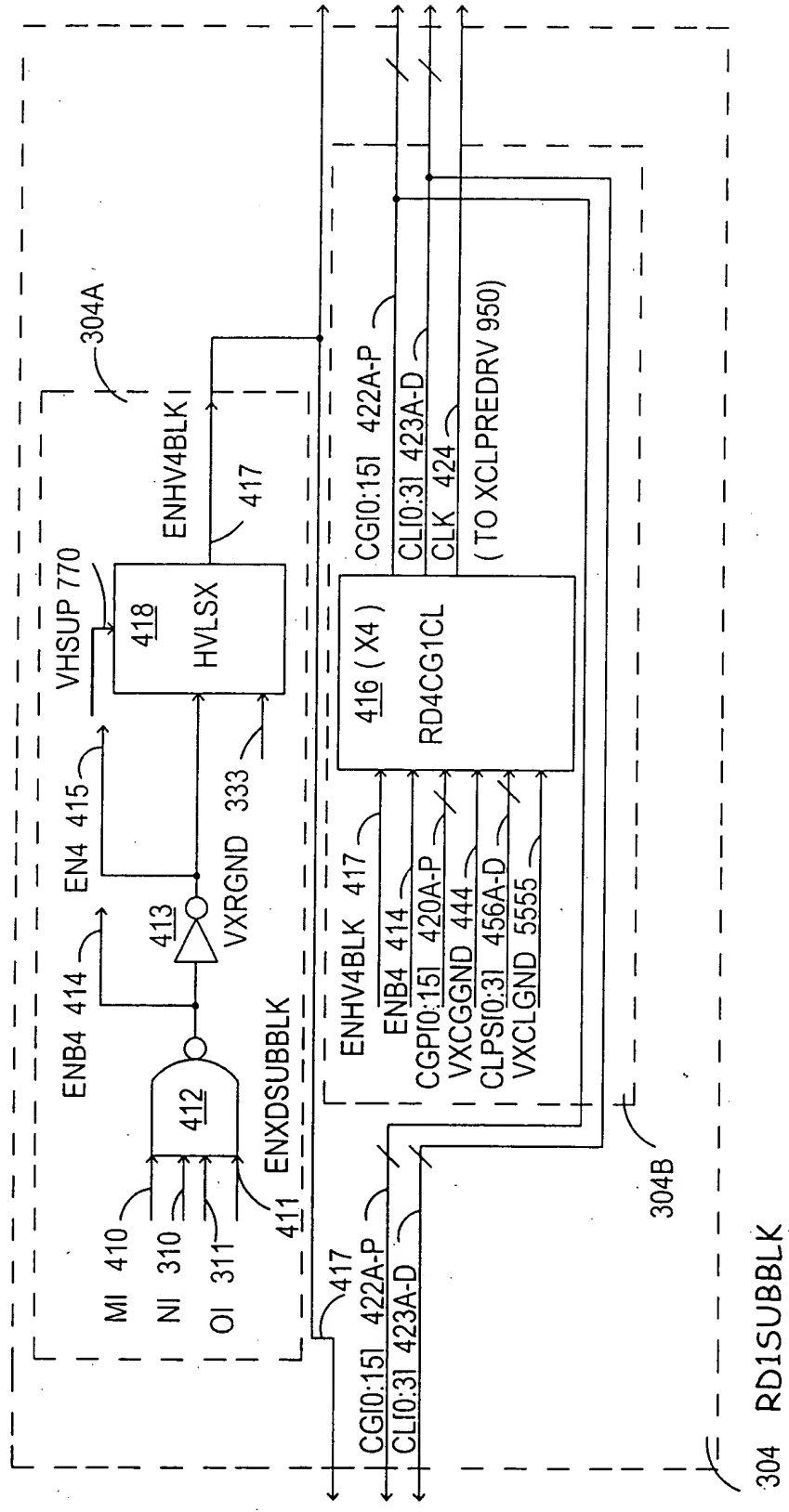


FIGURE 10

TOP OF PAGE 245260

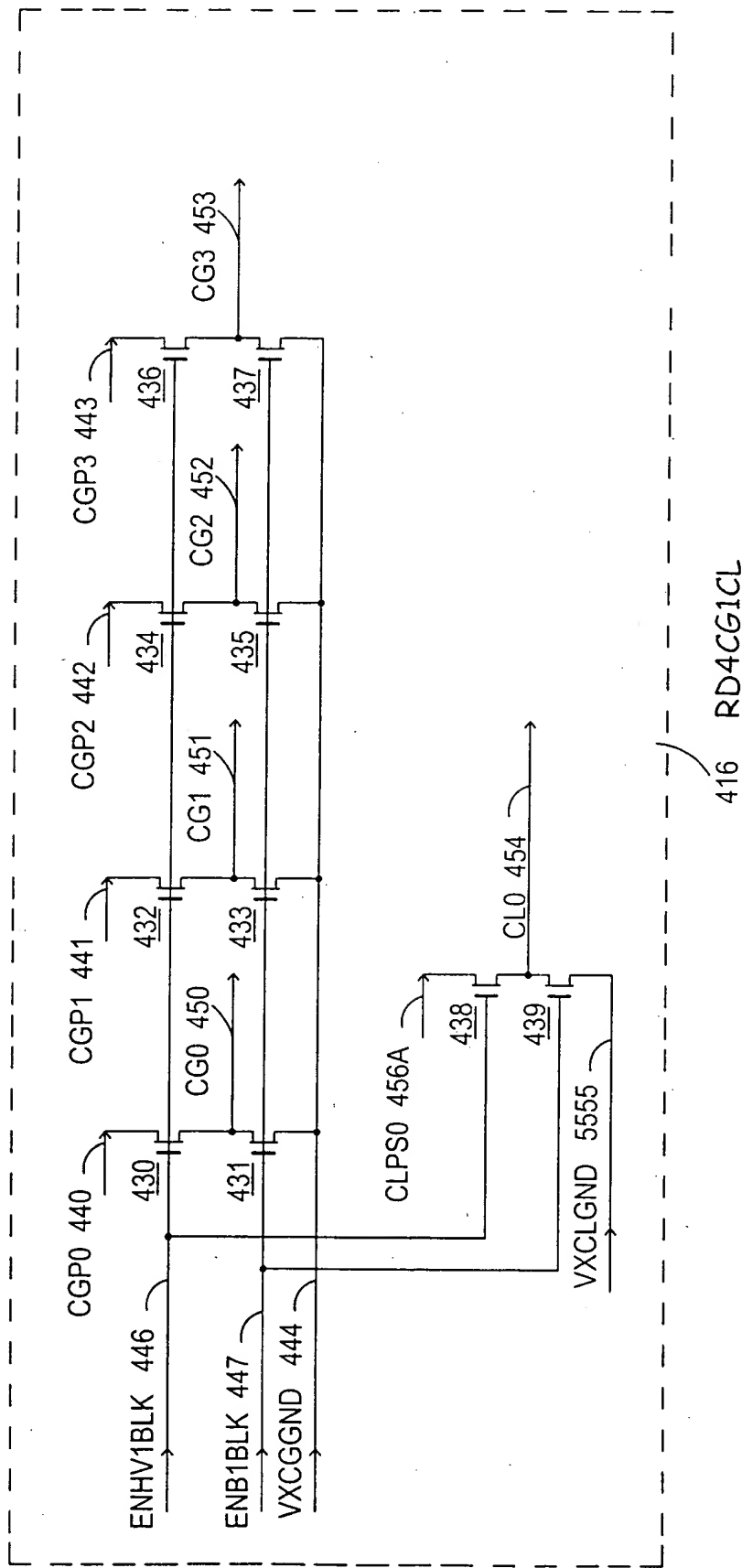
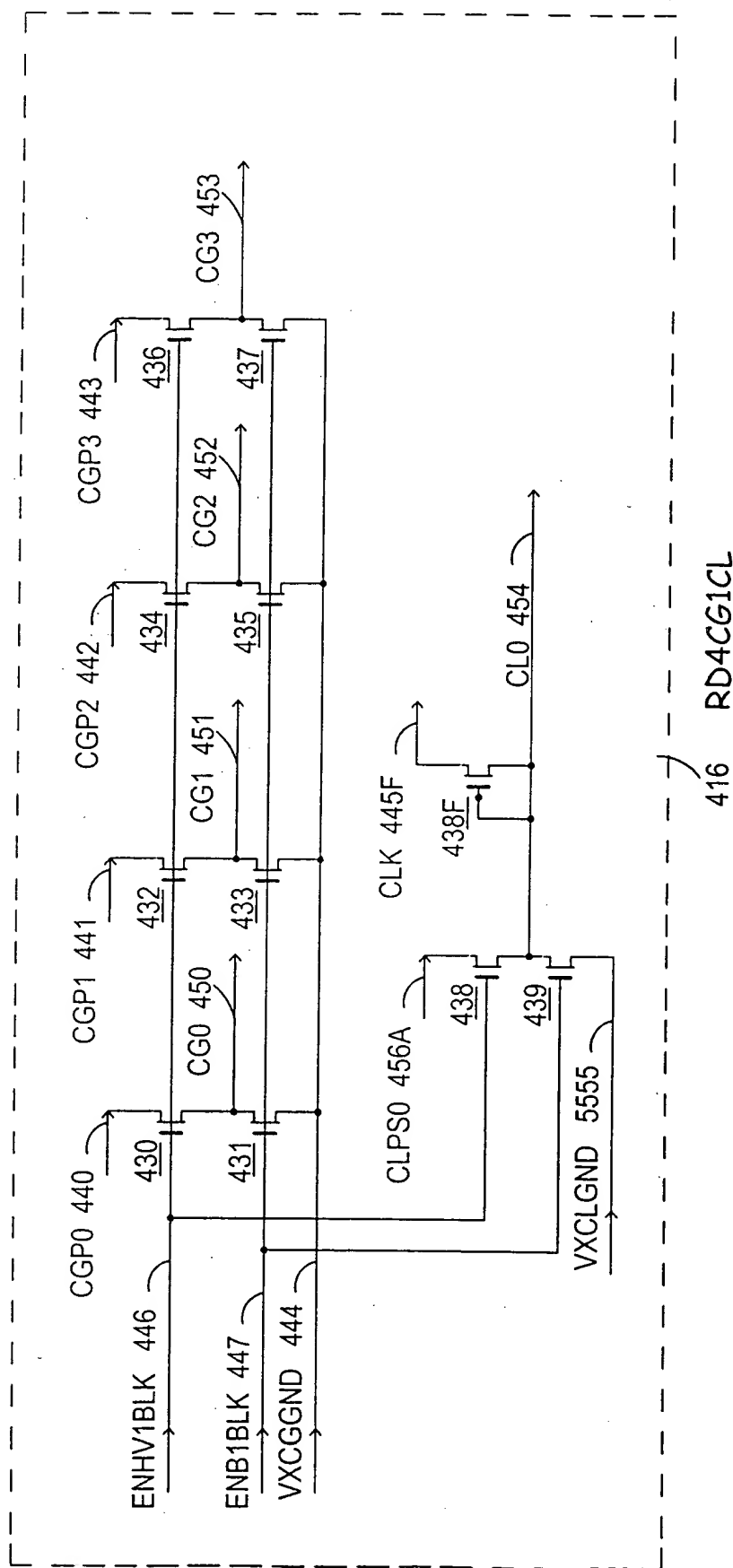
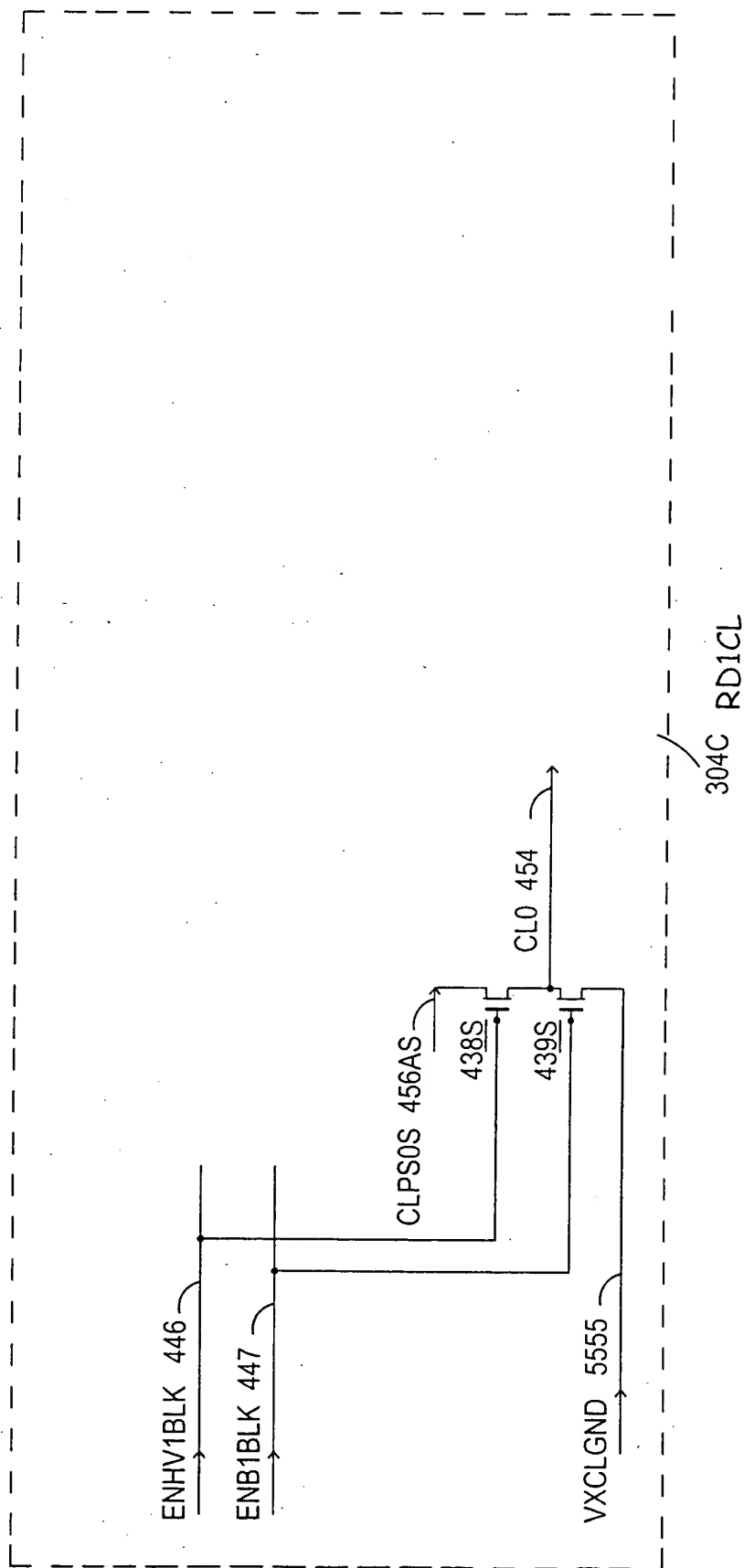


FIGURE 11A



**FIGURE 11B**



**FIGURE 11C**



FIG. 12

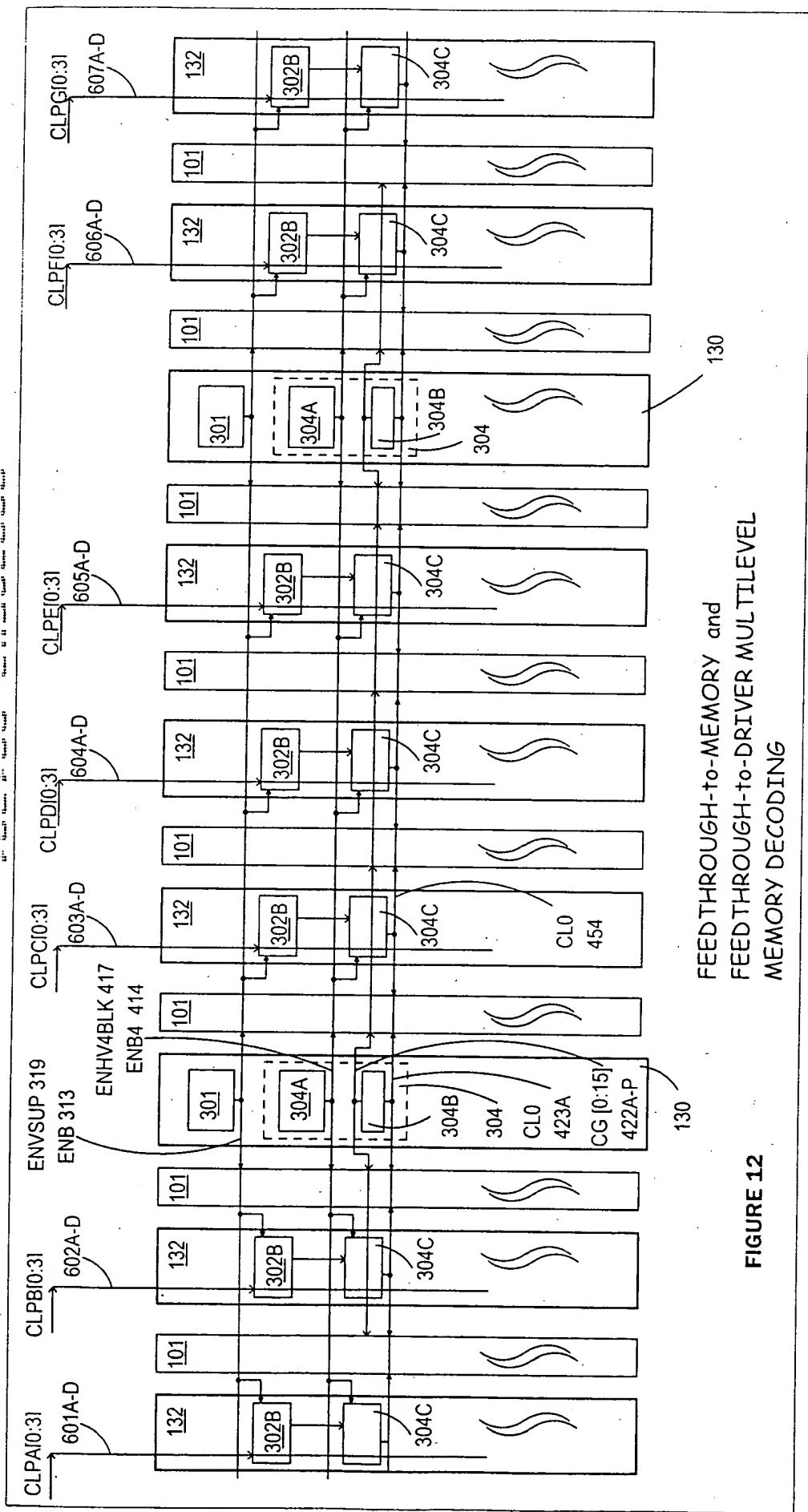
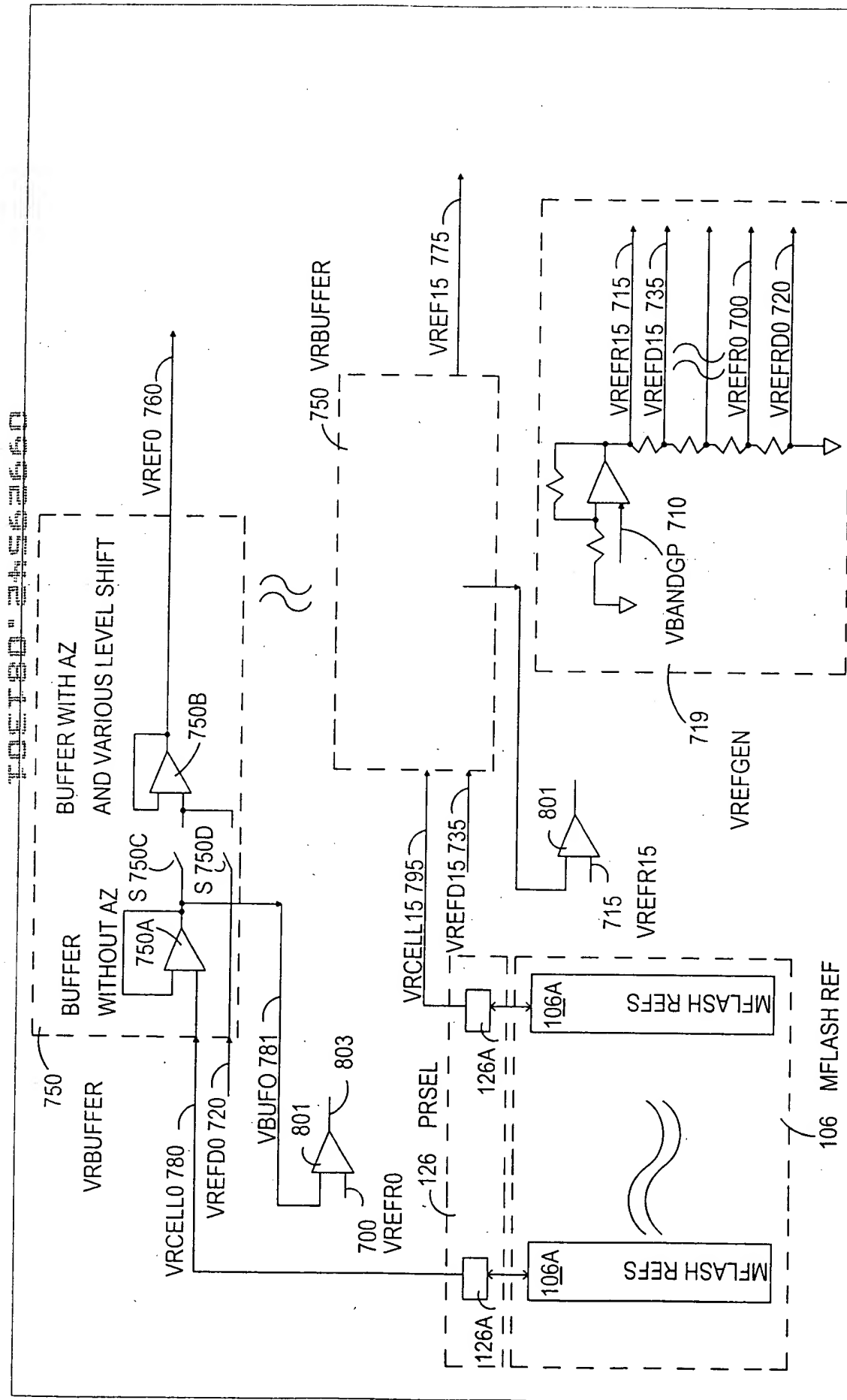


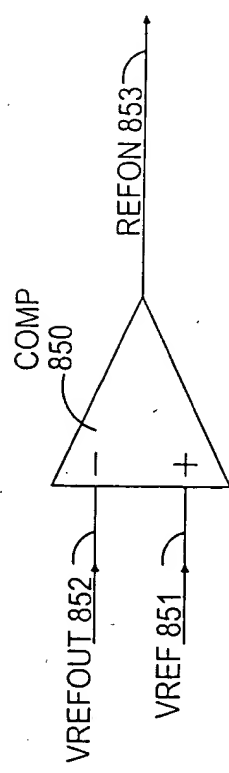
FIGURE 12





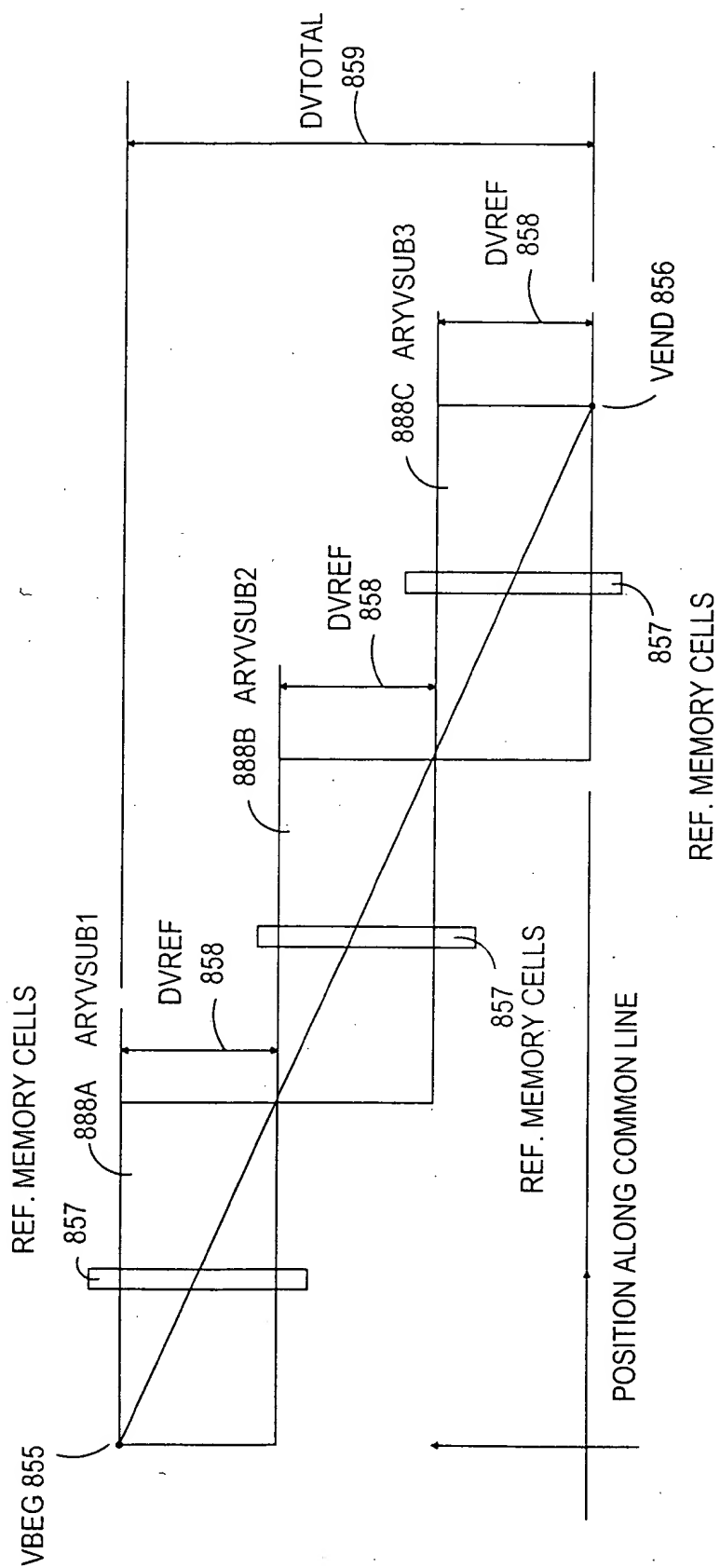
## FIGURE 14

TOP SECRET



REFERENCE DETECTION

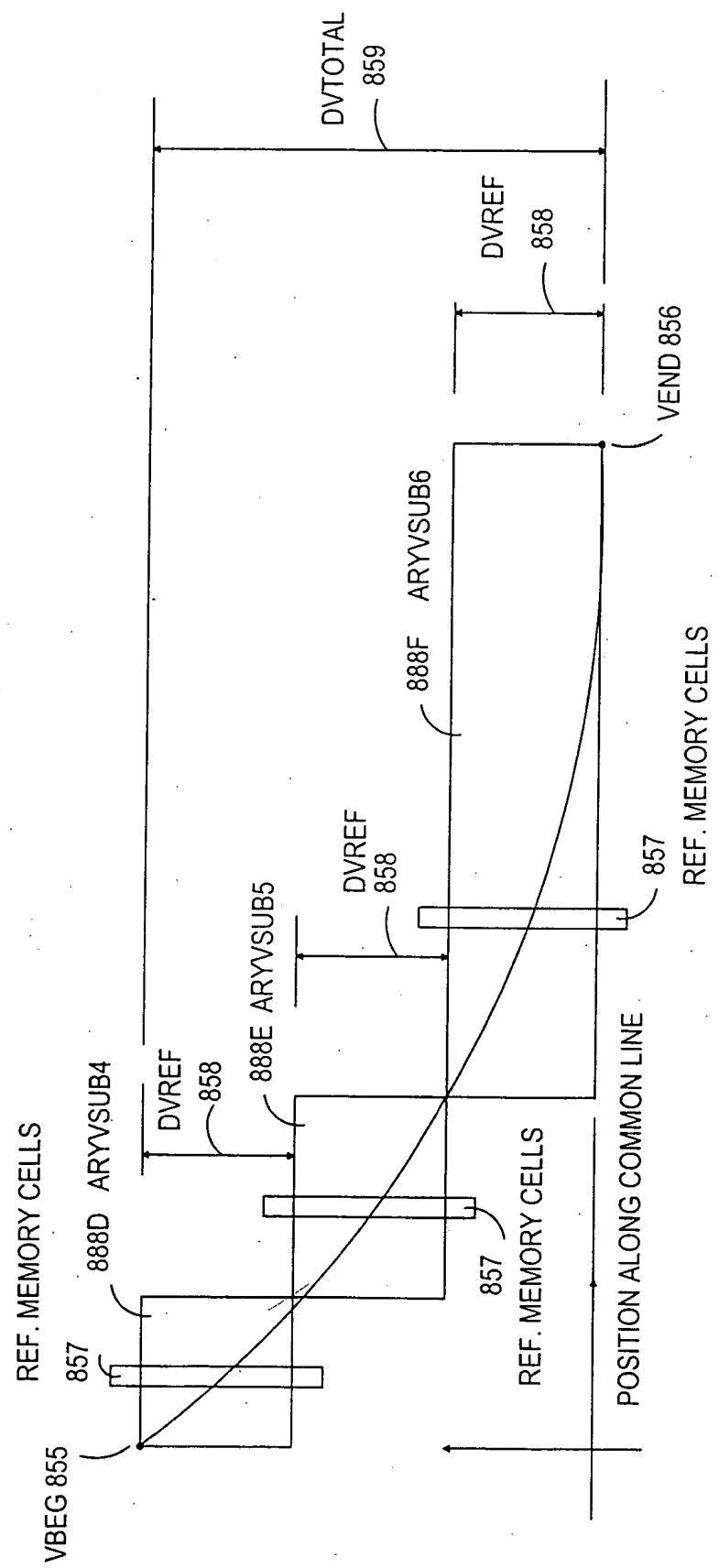
FIGURE 15



**FIGURE 16**

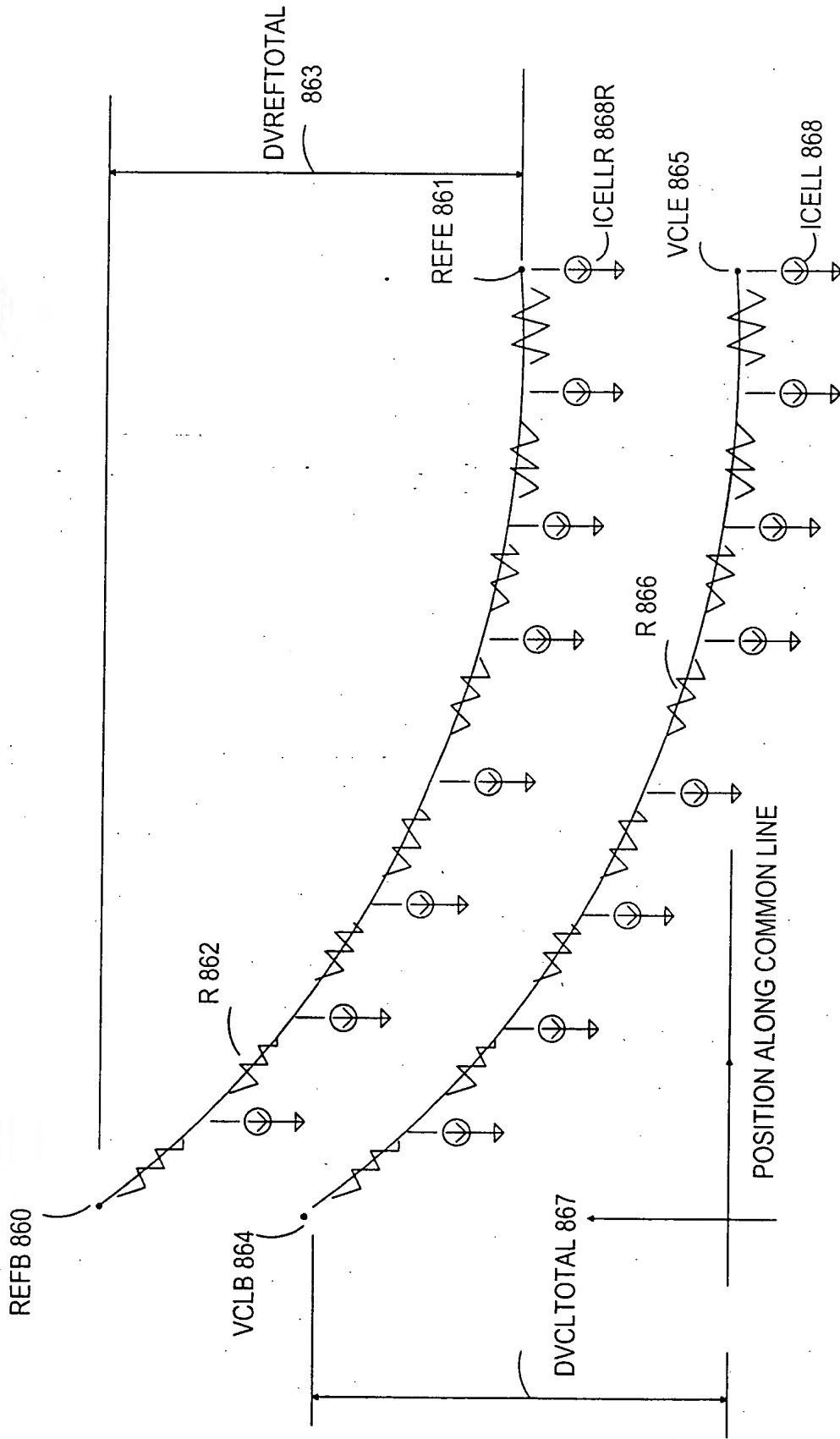
# POSITIONAL REFERENCE SYSTEM: LINEAR

REF. MEM. CELLS



POSITIONAL REFERENCE SYSTEM: GEOMETRIC

FIGURE 17



REFERENCE SYSTEM: GEOMETRIC  
COMPENSATION

FIGURE 18

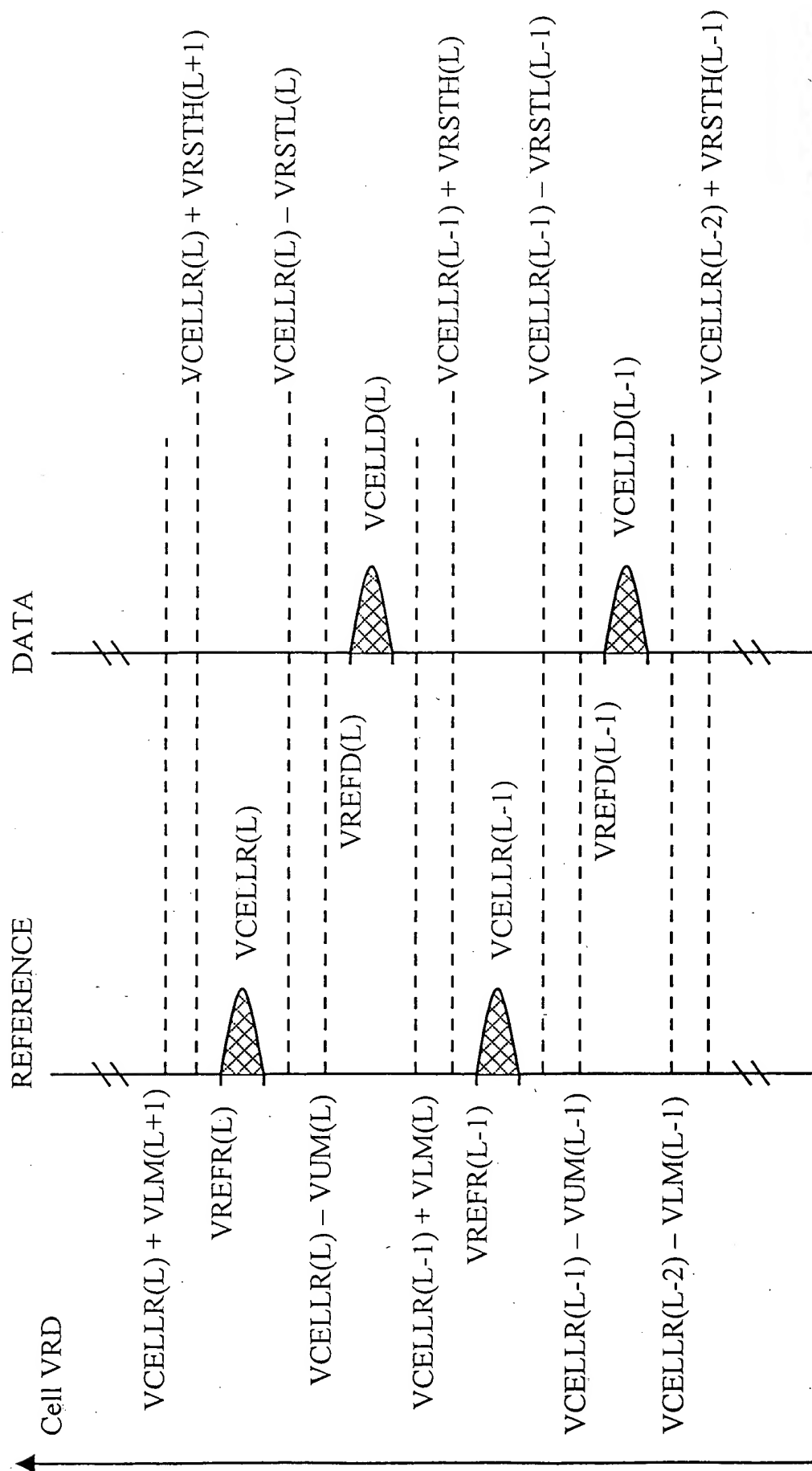


FIG. 19A



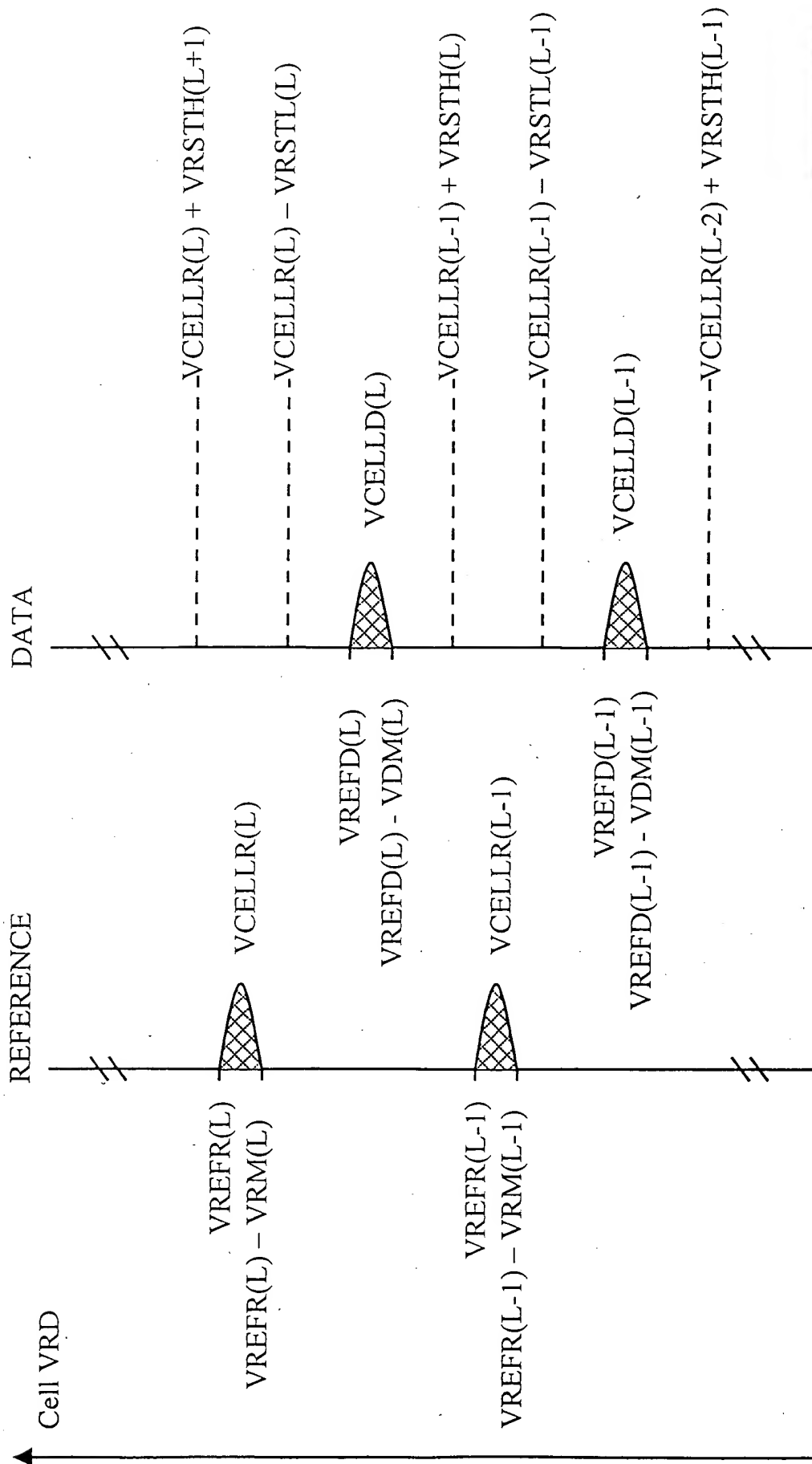
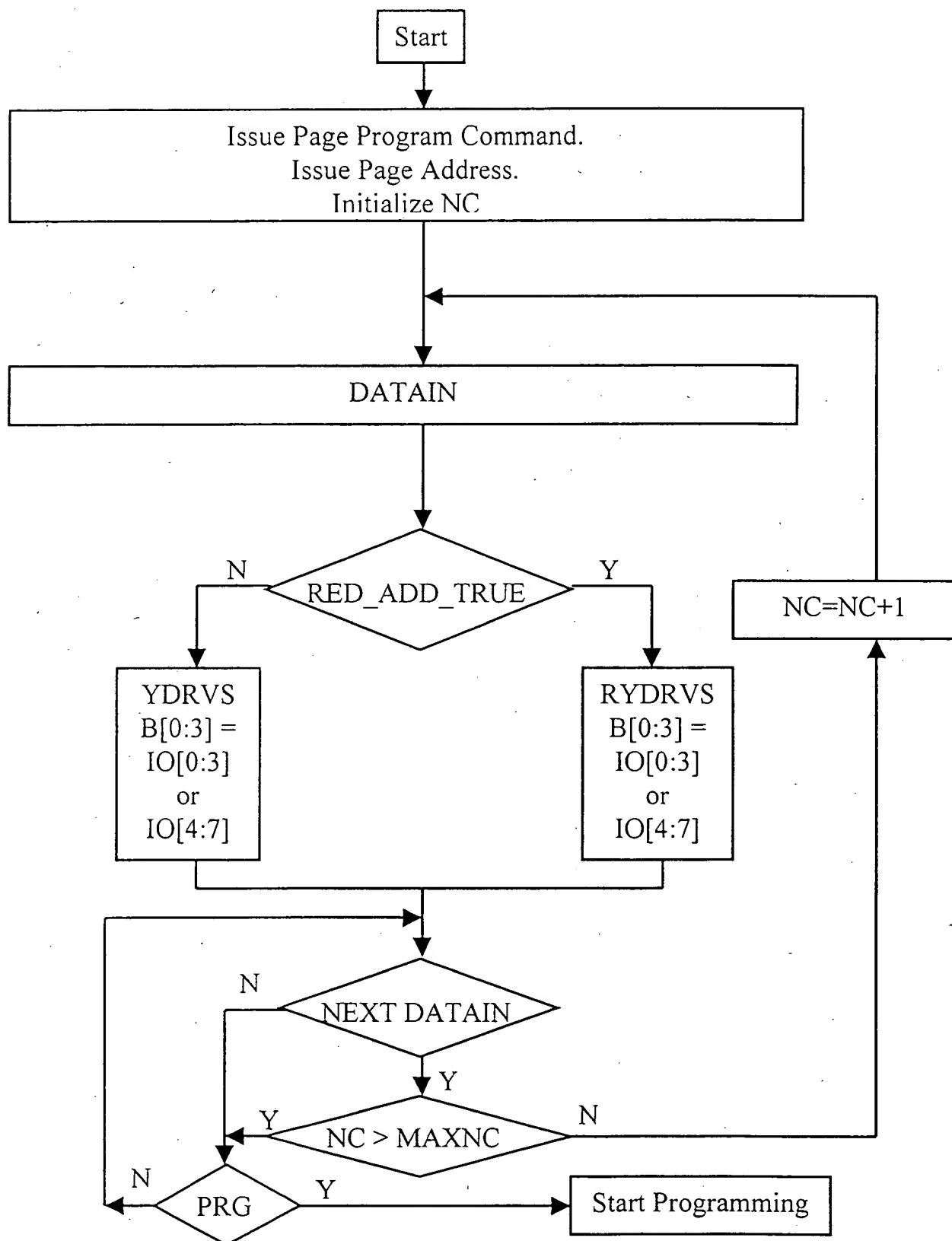
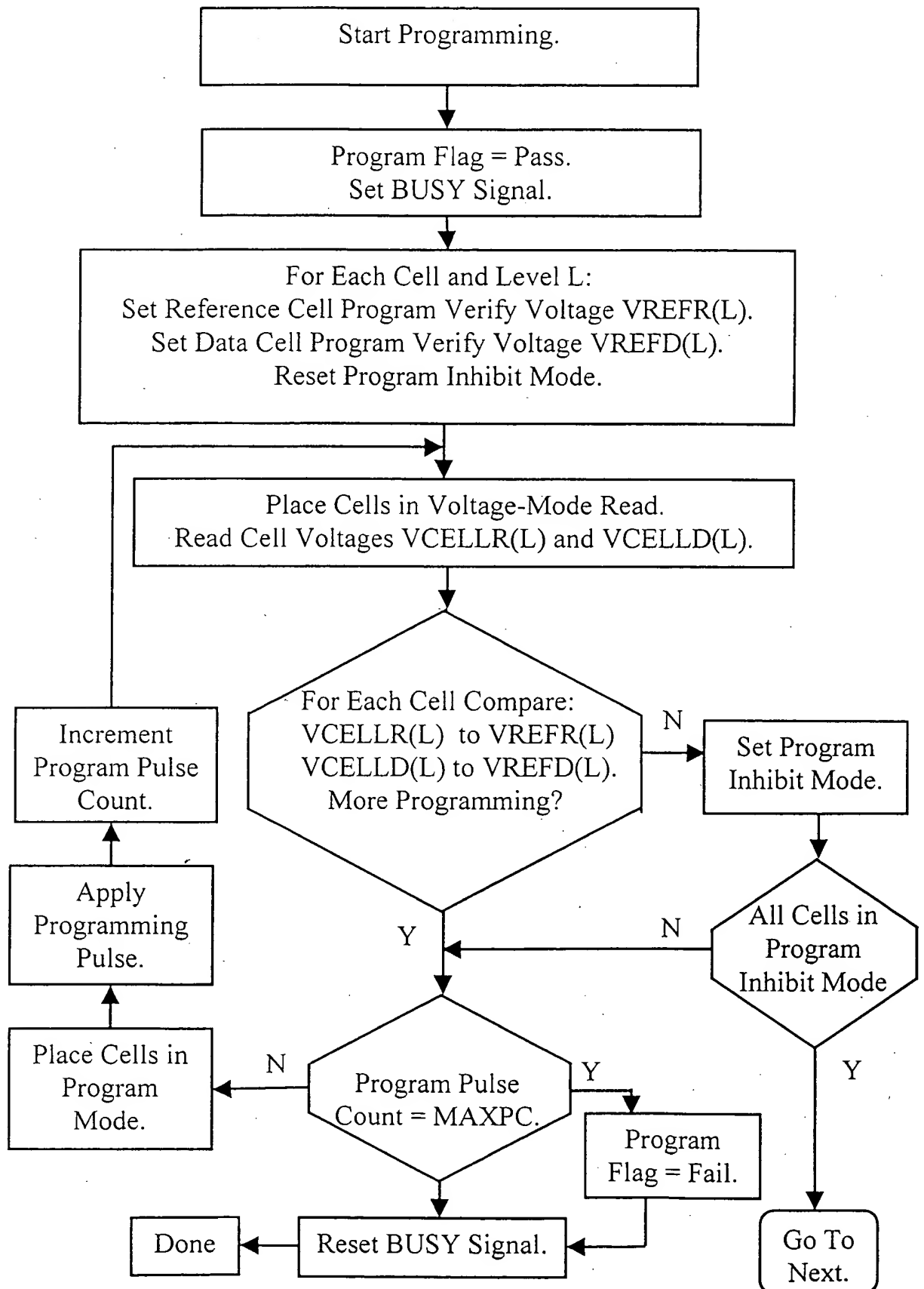


FIG. 19B





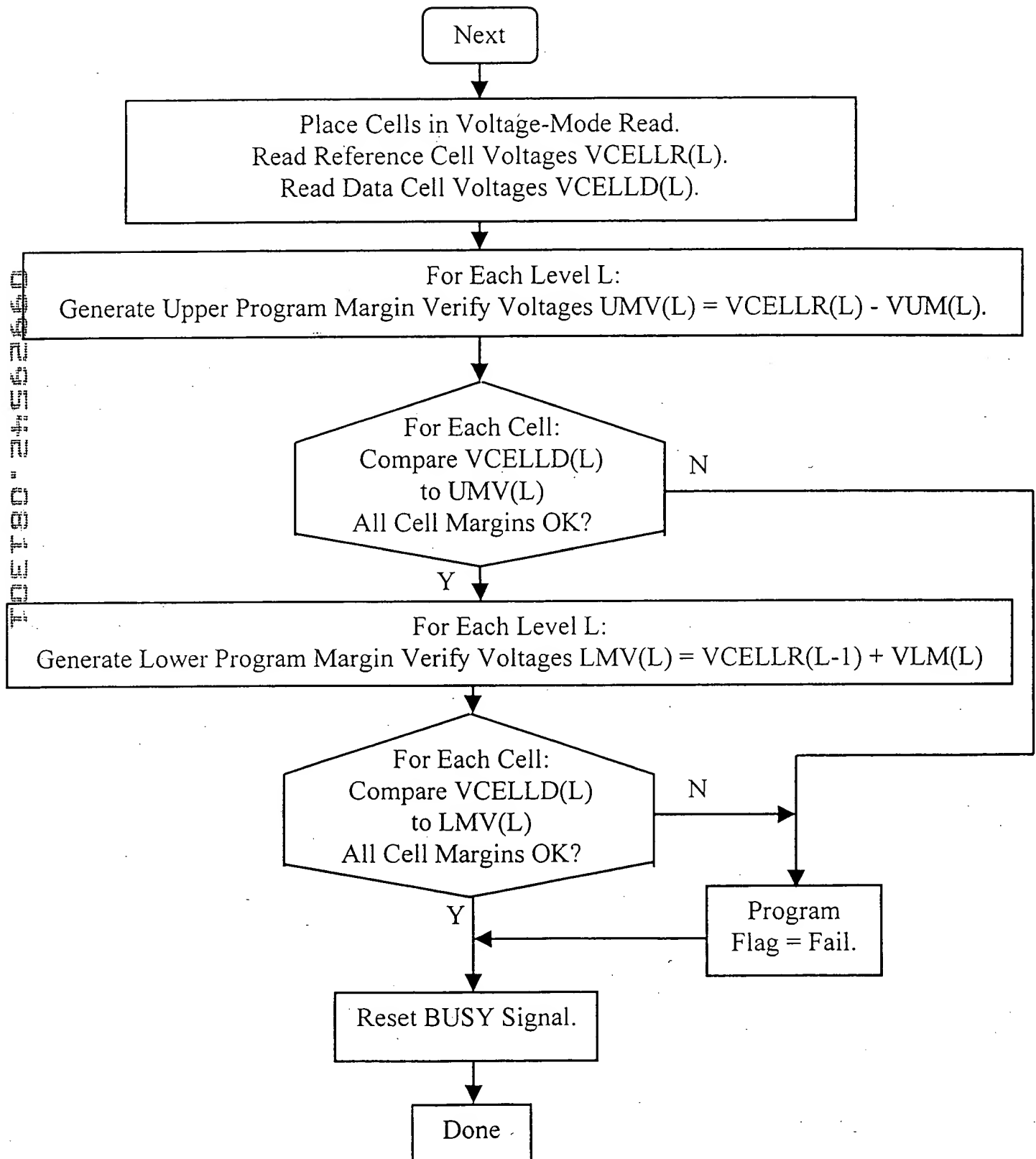
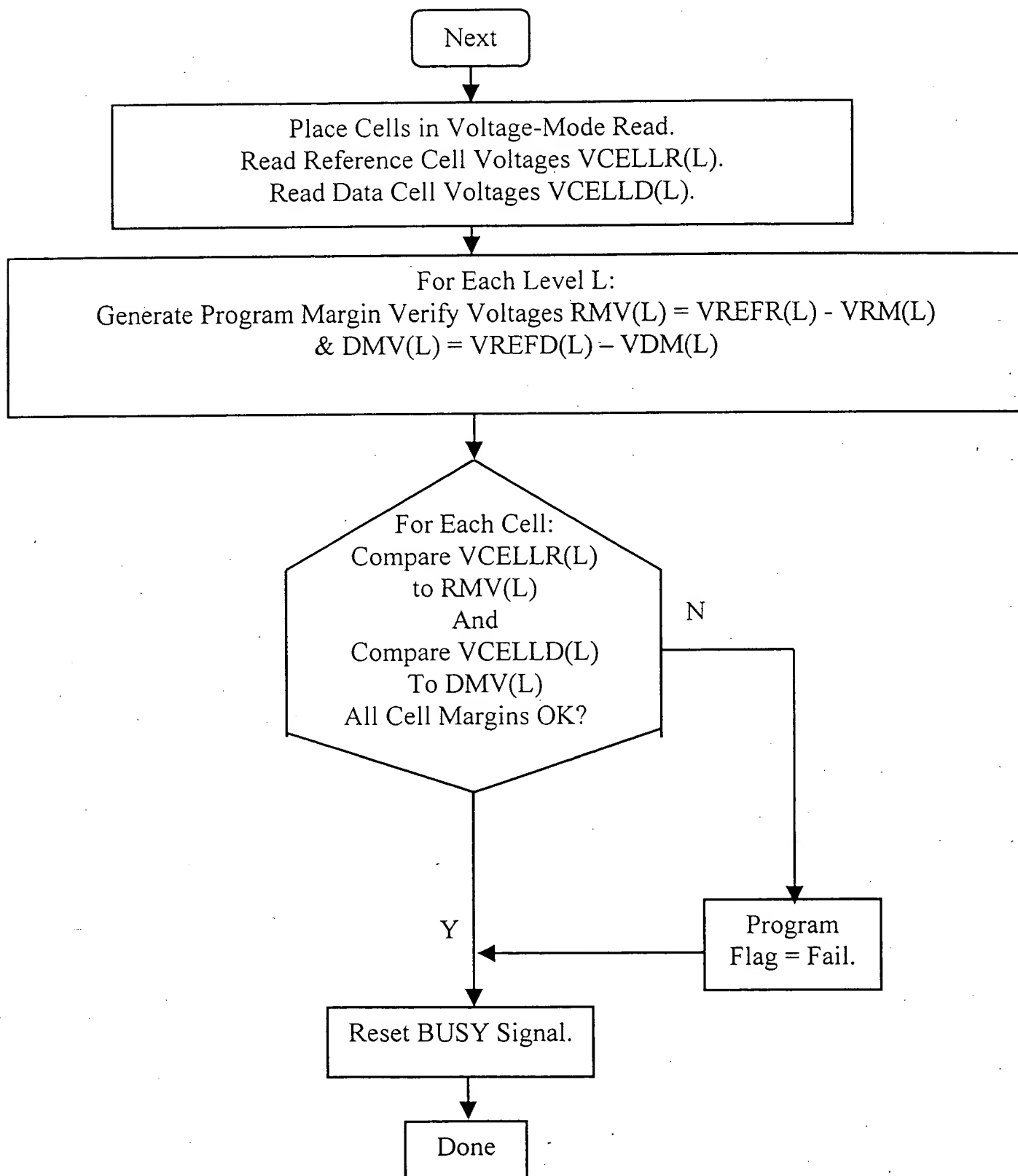
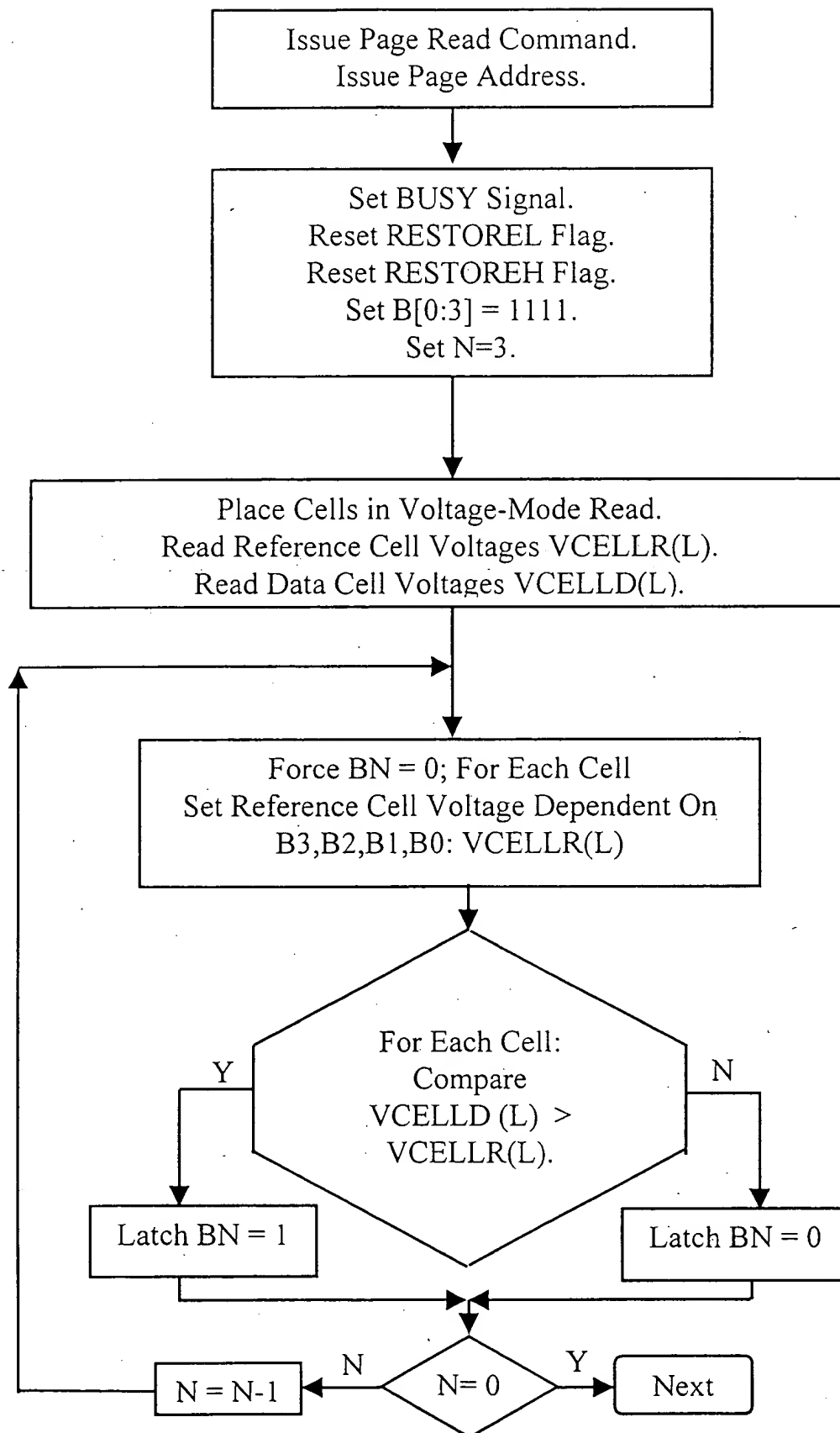


Fig. 22A



**Fig. 22B**



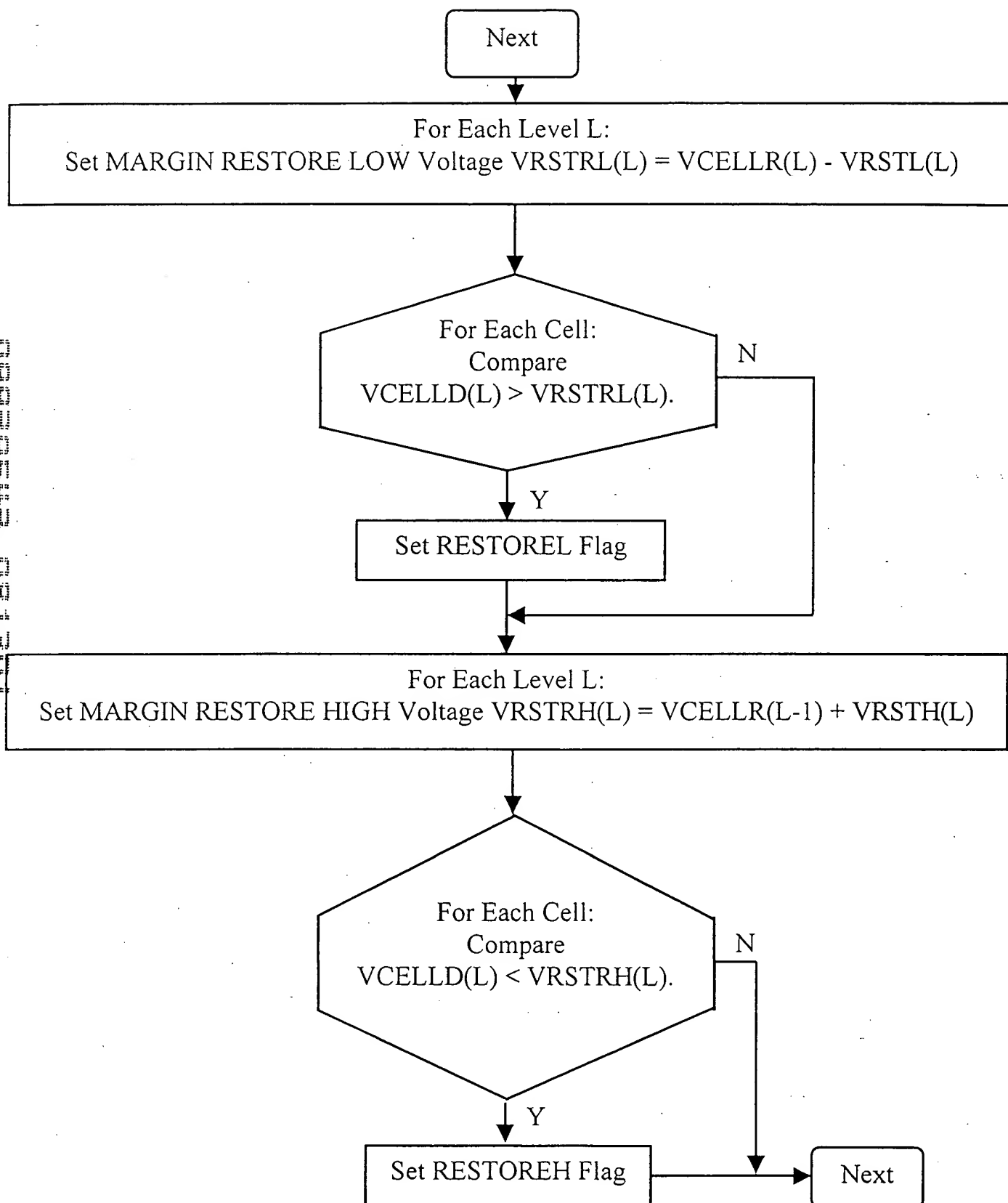


FIG. 24

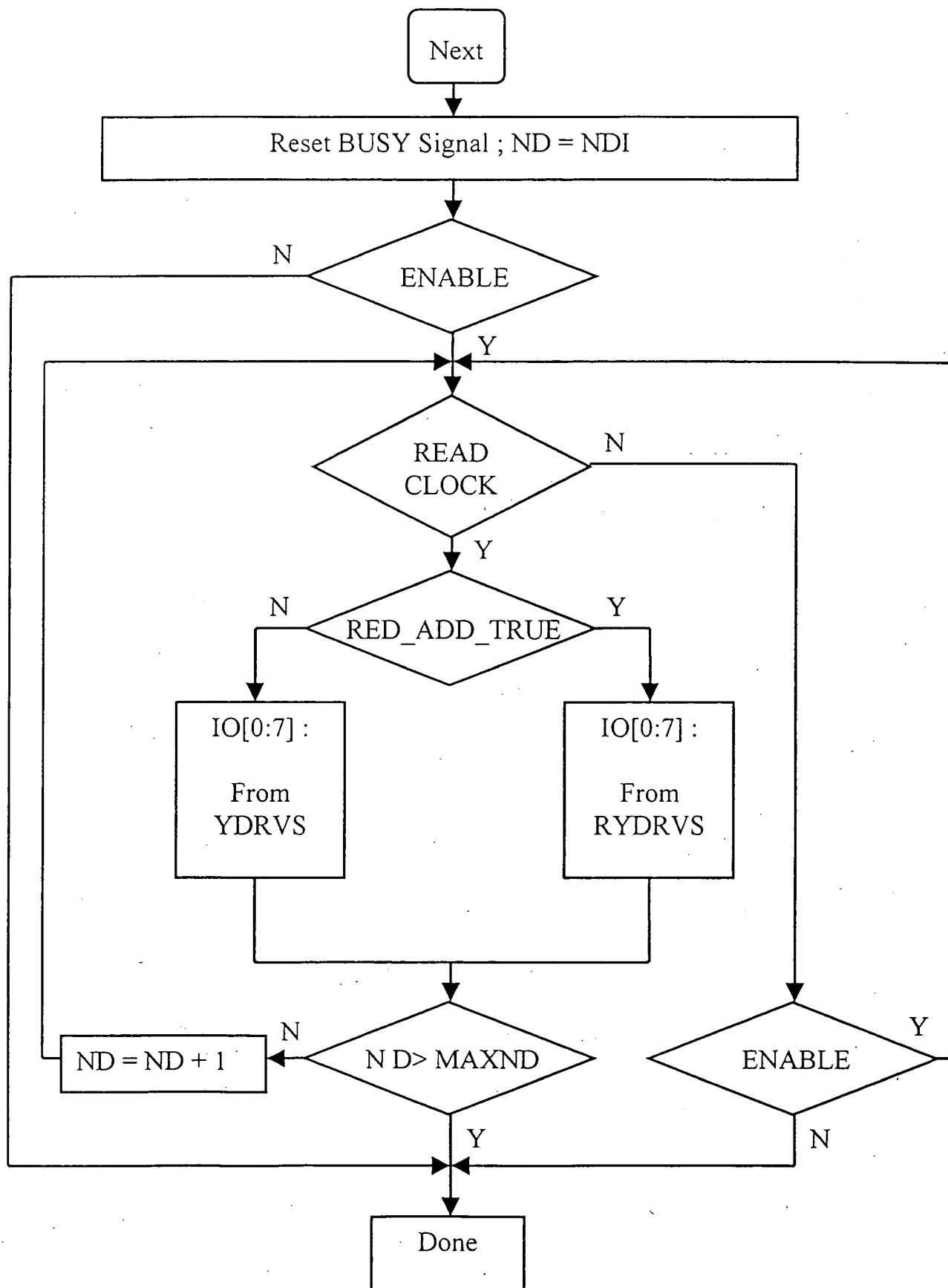


FIG.\_25



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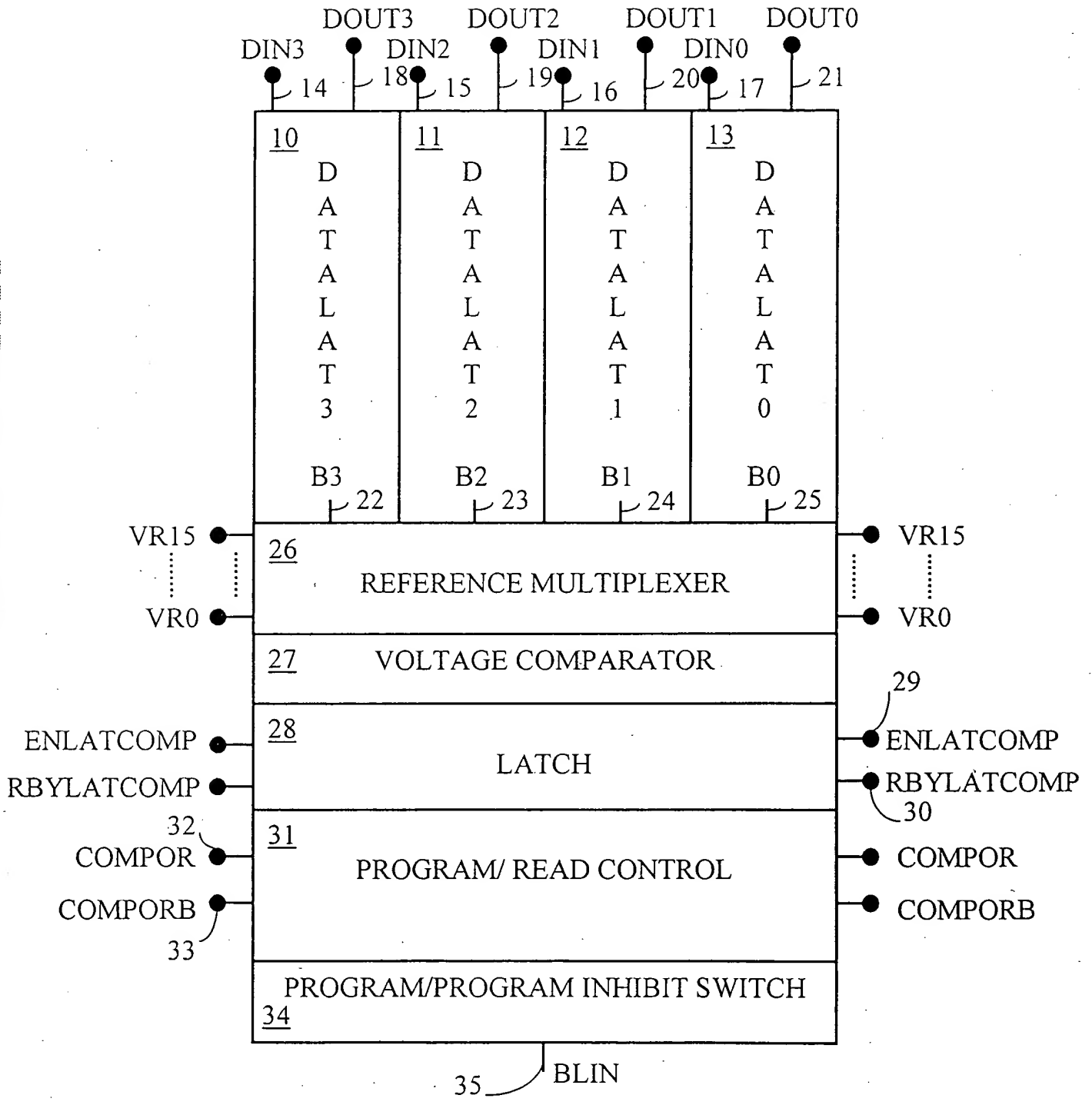


Fig. 26

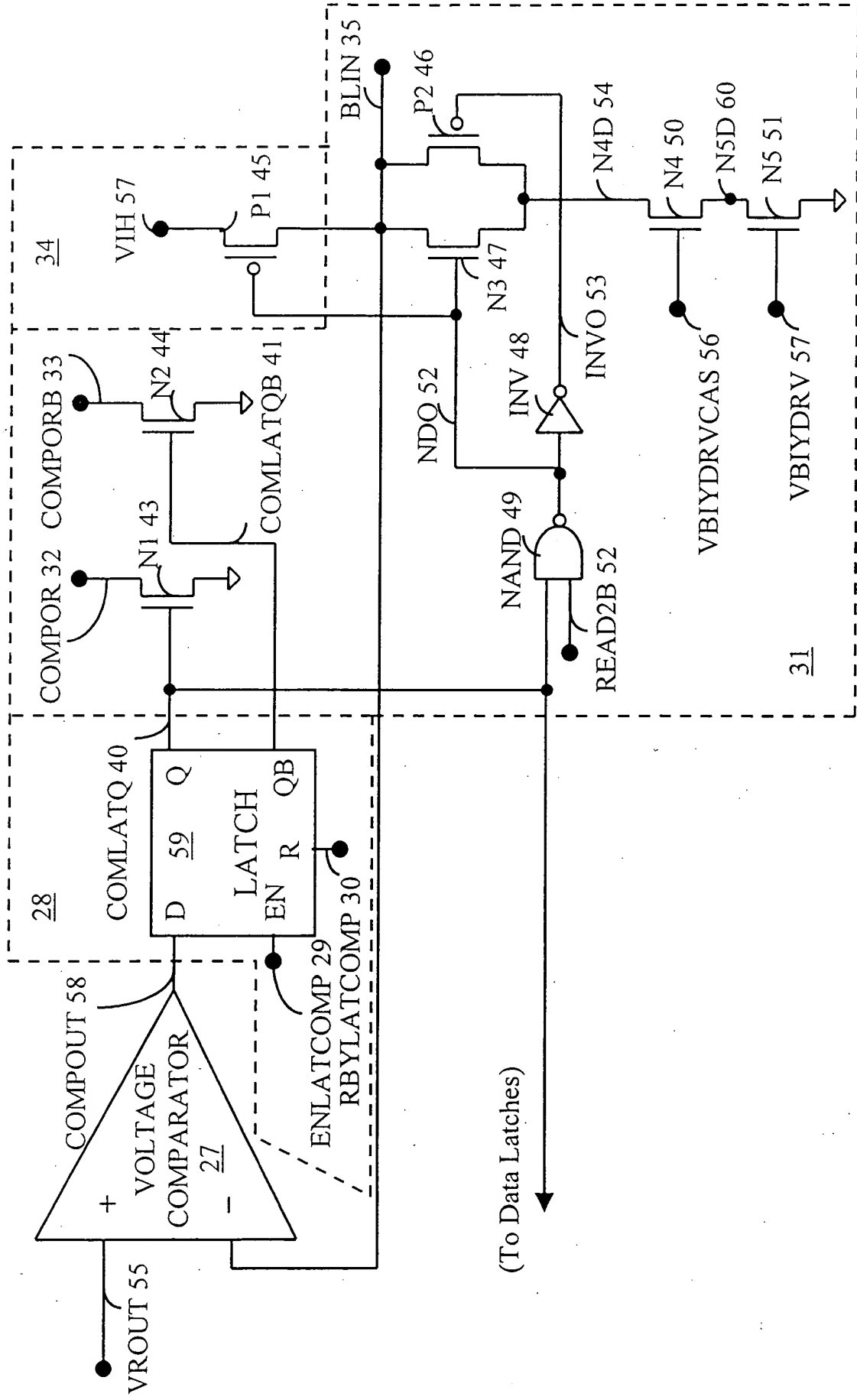


Fig. 27